Simulation of Half-Center Oscillator Circuits Employing Newly Developed Models of Fabricated Memristors

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***Abstract*— This work aims to demonstrate the utilization of fabricated memristors in bioinspired analog circuits. To this end, two types of memristors of the structures Pt/TiO_2/TiO_x/Pt and Au/TiO_2/TiO_x/Au have been fabricated and characterized. The current-voltage measurement results were used to derive models for these devices both through curve fitting using MATLAB and consulting models proposed by other groups. A Verilog-A model was developed for modelling our fabricated memristor, which was used in Cadence Spectre simulations of an analog weak inversion Half Center Oscillator (HCO) circuit. The simulations show, through comparison of HCOs employing our memristors, linear resistors and no memristors or resistors, that the varying resistance of memristors create a dynamic damping effect and result in the modification of oscillation amplitude, rhythm and improved cycle stability.**

Keywords—memristor, modelling, resistive switching, half center oscillator, weak inversion analogue circuits

I. INTRODUCTION

Memristors are nanoscale electronic devices which establish a relationship between flux and charge and are considered as the fourth passive circuit element [2]. Since flux is the time integral of voltage and charge is the time integral of current, memristor provides a time integral relationship between voltage and current, like resistors (resistors relation independent from time and rate of change of voltage and current). For these devices, ratio between voltage and current called memristance which is shown with the letter M. Memristance is instantaneous resistance of device which is a function of charge(q). This relation can be expressed as in (1) and (2) [2]:

$$V(t) = M\big(q(t)\big)i(t) \quad (1)$$

Where:

$$M(q) = d\varphi(q)/dq \quad (2)$$

The circuit design process relies heavily on circuit simulations. Circuit simulators such as Simulation Program with Integrated Circuit Emphasis (SPICE) and Cadence Spectre use device models to enable accurate circuit analysis.

A generalized model of the memristor has not been established yet. Therefore, in order to utilize and benefit from memristive properties in analog circuits, accurate and practical models are required.

Research groups have proposed different models of existing devices in various material combinations for example the model proposed for $Pt/TiO_x/TiO_2/Pt$ devices by Jeong et. al. [3] and the "memdiode" model by Blasco et. al. [4]. In an effort to attain a generalized memristor model, Miranda et. al. have suggested that these types of devices can be modelled like an anti-parallel connected diodes series connected to a memristor and went onto improving their models such that they are convenient to use in simulations [4-6]. In this model, device shows exponential behavior similar to a diode when it is in high resistance state, after reaching a set voltage, it shows a linear behavior when it is in low resistance state.

With the increasing interest in memristors, new areas of application have been investigated. Various studies have shown that the memristor can be used in artificial synapse-like structures, artificial neural networks, and bio-inspired analogue circuits [7][8].

This work focuses on utilizing memristive dynamics in a certain bio-inspired circuit: Half Centre Oscillator (HCO). The HCO circuit investigated in this paper was proposed by Nakada et. al. [9], coupling four of these HCO blocks to one another make up a Central pattern Generator (CPG) which mimics rhythmic activity of a four-legged animal such as walking, running. Two distinct topologies of these circuits have been shown to exhibit variation in amplitude and rhythmic variation as well as cyclic stability when they employ memristors [10]. This paper aims to show the

development of models of our own fabricated memristors and these memristors being used in the HCO circuit.

This work focuses on modelling fabricated memristors by our group, in the structures of $Au/TiO_x/TiO_2/Au$ and $Pt/TiO_x/TiO_2/Pt$ and using these models in HCO circuits.

To achieve this, we use measurement results obtained from our own devices to create phenomenological models through curve fitting. The equations that were developed through this endeavor was then compared to existing memristor models. As a result, we developed SPICE and Verilog-A models of our devices.

Our motivation is to contribute to the development of a generalized memristor model and employing memristors in bioinspired analogue circuits.

II. Device Fabrication

$Au/TiO_2/TiO_x/Au$ devices were fabricated on a $Si+SiO_2$ wafer. Both top and bottom electrodes are Au. Cr was used as an adhesion layer for Au, 5nm Cr was deposited by E-beam evaporation. 40nm Au was deposited using thermal evaporation. Electrodes were patterned using a negative photoresist and lift-off was performed. The active layer consists of stoichiometric TiO2, deposited through sputtering a TiO_2 target, and doped TiO_x. TiO_x layer was attained by sputtering a Ti target while allowing in 5% O_2 plasma into the chamber along with Argon, similar to what is described in [11]. This layer is patterned using a positive photoresist. Finally, Cr+ Au is deposited again through thermal evaporation and patterned by liftoff.

$Pt/TiO_2/TiO_x/Pt$ were fabricated similarly: on a $Si+SiO_2$ wafer with Pt top and bottom electrodes. Cr (20nm) is used as an adhesion layer for Pt (7nm). Electrodes are patterned with a negative resist and through liftoff. The active layer is fabricated following the same process as described above. Both structures are depicted in Fig.1 .

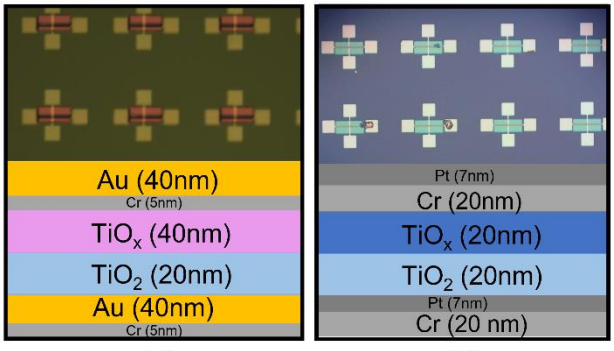

Fig.1 *Fabricated Memristor microscope photos and cross-section diagrams showing layers (a) $Au/TiO_2/TiO_x/Au$ device (b) $Pt/TiO_2/TiO_x/Pt$ device*

III. Measurements

Au electrode memristor was driven by 100µA, 25mHz triangular current source with 100ms delay and 1µA interval, the resulting output, memristive voltage was measured. Measured voltage data, input current data vs. time given at Fig.2 and I-V graph given at Fig.3

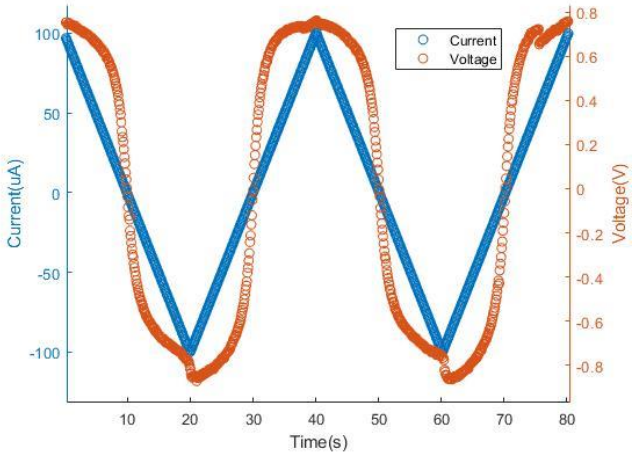

Fig.2 *Measured data of I, V vs. T of Au electrode memristor*

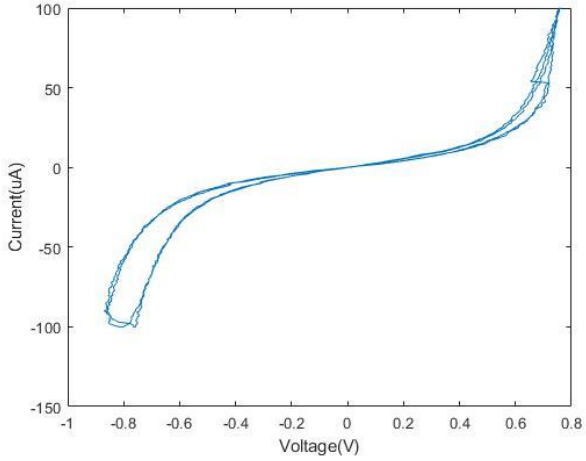

Fig.3 *I-V graph of Au electrode memristor*

Pt electrode memristor was driven by 2V, 40mHz triangular voltage source with 62.5ms delay and 20mV interval, current trough memristor measured. Measured current data, input voltage data vs. time given at Fig.4 and I-V graph given at Fig.5

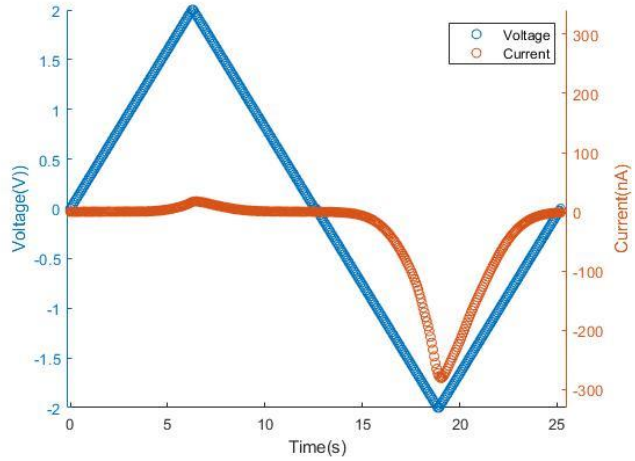

Fig.4 *Measured data of I, V vs. T of Pt electrode memristor*

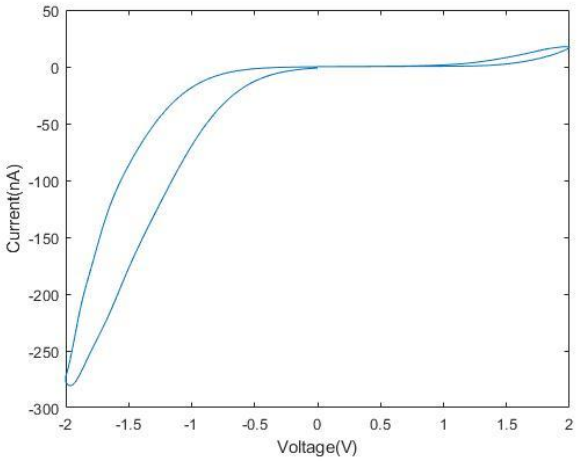

Fig.5 *I-V graph of Pt electrode memristor*

IV. Curve Fittings

In this work, curve fitting is used to obtain memristance and current/voltage equations and attaining a continuous model for our memristors.

Firstly, Au electrode memristor model's memristive behavior is analyzed as a piecewise function and curve fitting is applied to the memristive response corresponding to the upward and downward slopes of the input signal. For each slope a 4th degree Gaussian (in the sum of terms of $ae^{-\left(\frac{t-b}{c}\right)^2}$) curve fit has been applied. R-square value was over 99% for each fit pointing to a reliable fit. Fitted curve compared with measured voltage data given at Fig.6

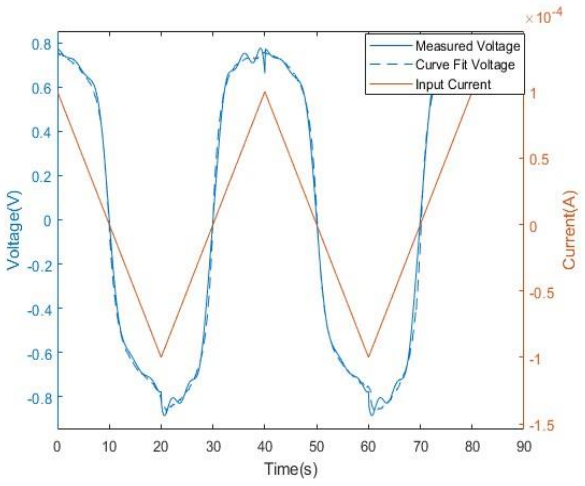

Fig.6 *Au electrode memristor fit model for voltage*

The Pt electrode memristor was excited with a voltage signal. Curve fitting was applied to the measured memristive current flowing through the device for negative and positive parts of voltage. Similar to the analysis of the Au electrode memristor, 4th degree Gaussian curve fit has been utilized. Fitted curve compared with measured current data given at Fig.7.

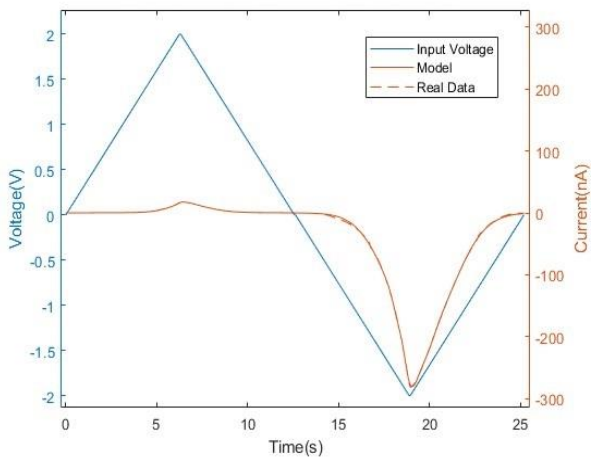

Fig.7 *Pt electrode memristor fit model for current*

V. Modelling

Saludes-Tapia et.al suggested a general model for devices which behave as memdiodes named Quasi-Static Memdiode Model (QMM). Using the QMM model, devices of different structures have been modelled successfully [6]. The QMM model's I-V relation is given in (3).

$$I(V) = I_0(\lambda)\, sinh(\alpha(\lambda)[V_c]) \qquad (3)$$

$I_0(\lambda)$ represents current amplitude factor function, $\alpha(\lambda)$ represents fitting parameter amplitude function, λ is state variable and V_c represents voltage between terminals of memristive device.

In this model, when the state variable is 0, the device current changes in the low resistance region, that is, in the exponential (sinh) region. Then, when the state variable comes to the set curve, that is, it increases towards 1, while the device current transitions from the low resistance region to the high resistance region, that is, the linear region. Then, when the state variable stays 1 until a certain voltage, when it comes to the reset curve, that is, it drops towards 0, the device current comes back to the low resistance region and starts to exhibit exponential (sinh) movement. This creates the hysteresis loop. Fig.8 shows this hysteresis loop and current with sinusoidal voltage versus time. Fig.9 shows state variable vs. voltage between terminals.

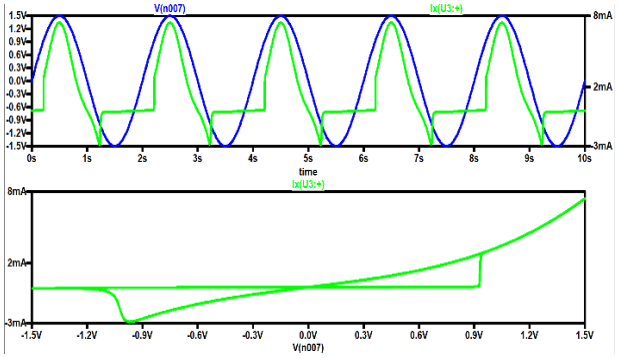

Fig.8 *QMM model I-V graph. (Green-I, Blue-V)*

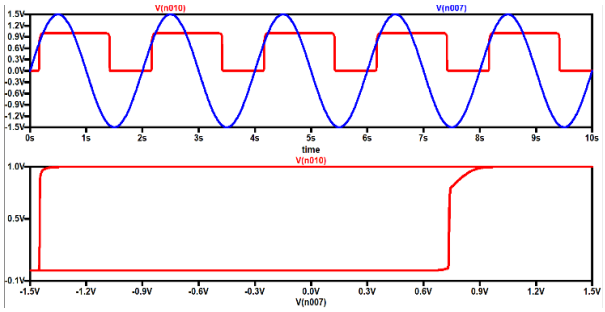

Fig.9 *QMM model λ-V graph. (Blue-V, Red- λ)*

We observed that our devices' voltage, current and state variable characteristics are compatible with the QMM model's equations. With these equations and changes in parameters we utilized the model in SPICE and created models in Verilog-A to be able to simulate circuits in Cadence Virtuoso environment.

The simulation results of the models of fabricated memristors in Verilog-A, models generated by curve fitting and measured data and can be seen at Fig.10 and Fig.11.

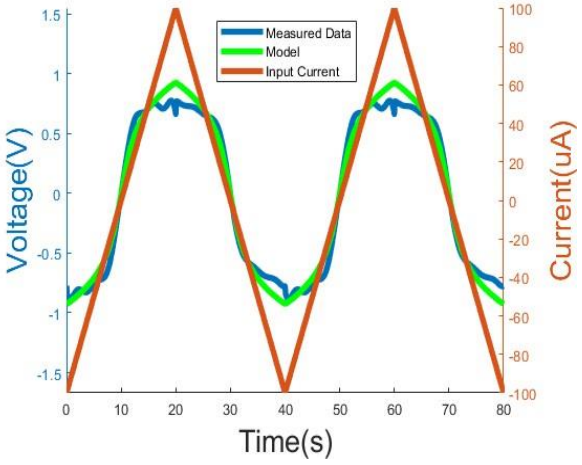

Fig.10 *Au electrode memristor model*

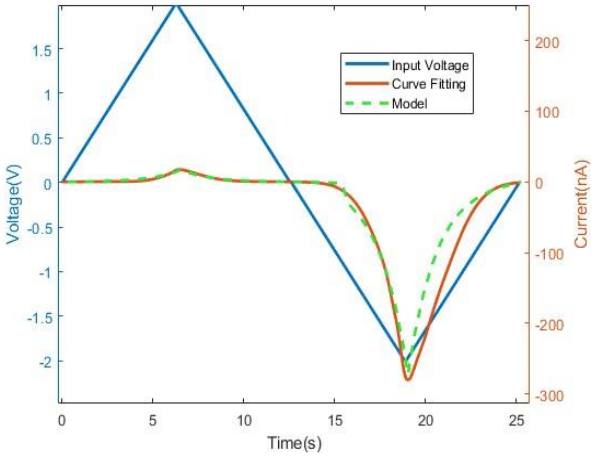

Fig.11 *Pt electrode memristor model*

VI. HCOs Employing Memristors

HCOs are blocks which consist of two neurons that do not fire individually but when coupled together, fire reciprocally. When two or more HCOs are coupled to one another they can mimic movement such as walking, trotting, and running of animals as demonstrated by Nakada et.al. [9].

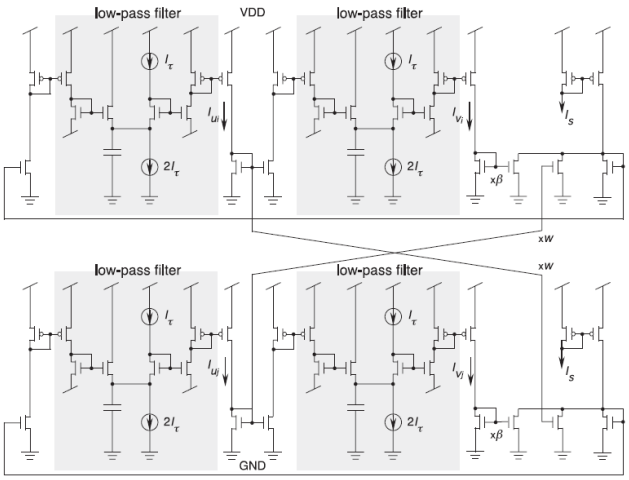

Fig.12 *Half Center Oscillator Circuit Schematic [9]*

As shown in the circuit schematic in Fig.12, the HCO consists of 4 low-pass filters and current mirrors. The top half of circuit called flexor half-center resembling neurons which activate flexor muscles and bottom half of circuit called extensor half-center resembling neurons which activate extensor muscles.

The HCO circuit produces 4 outputs named I_{ui}, I_{vi}, I_{uj} and I_{vj}. Here I_{ui} represents the inner state of i-th neuron and I_{vi} represents adaption variable of this neuron. Similarly, I_{uj} and I_{vj} belongs to j-th neuron which resembles extensor half-center which signals come after flexor half-center. By flexing then extending muscles the movement occurs. [9]

The circuit was simulated using the Cadence Virtuoso environment with the XFAB 0.35µm process. The transient response of outputs I_{ui} and I_{vi} can be seen at Fig.13, yellow line represents I_{ui} and blue line represents I_{vi}.

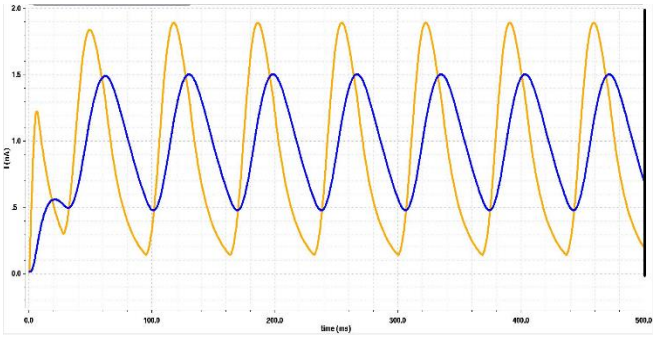

Fig.13 *HCO transient response*

To improve cycle stability and adjust the frequency of the output signals, we connect voltage driven memristors at transistor gates as in Fig.14

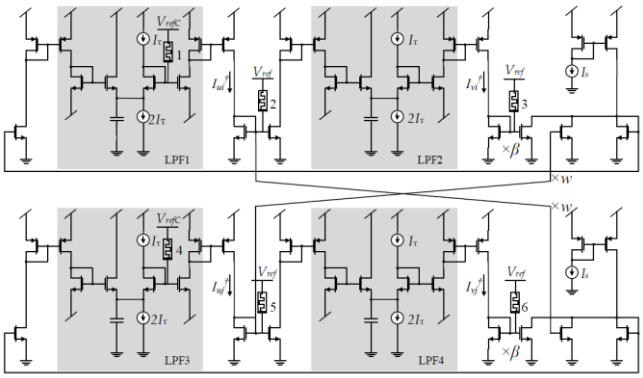

Fig.14 *HCO schematic with voltage driven memristors at transistor gates*

Simulations have been run for HCO without memristor (version seen in Fig. 12), HCO with 2 parallel connected Pt electrode memristors (schematic shown in Fig. 14) and HCO with 500MΩ linear resistors (resistors connected to the HCO in place of memristors shown in Fig. 14), which is about the same value of 2 parallel connected Pt electrode memristors average memristance. Phase portraits which allow us to see the stability and amplitude variation between outputs and inspects I_{vi} vs I_{ui} can be seen at Fig.15.

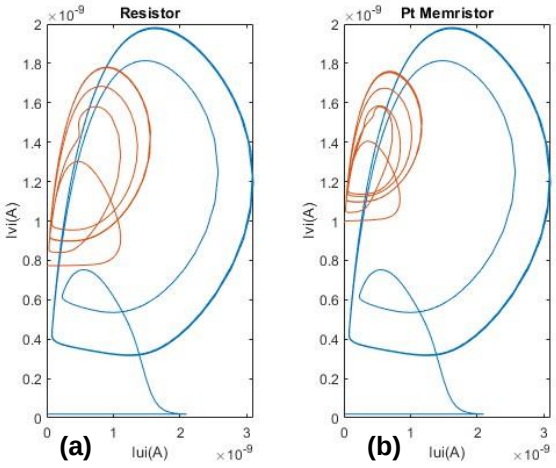

Fig.15 *Phase Portraits showing I_{ui} vs I_{vi}: a)Blue line – No Device, Orange Line- Resistor, b) Blue line – No Device Orange Line-Memristor*

After using Pt electrode voltage driven memristors in this circuit the amplitudes of I_{ui} and I_{vi} have shown a dynamic damping effect which resembles the amplitude can be adjusted through using memristors in circuit.

Also, gaps between cycles narrowed indicating stability of circuit improved. Frequency of outputs also changed with memristor. Frequency relation between outputs can be expressed as $f_{No\_Device}>f_{Resistor}>f_{Memristor}$.

So, if memristors are used in these circuits, frequency and amplitude of outputs can be adjusted while stability improved.

VII. Conclusion

Reliable and generalized device models are fundamental part of circuit design. We developed models of our own memristors to be able to simulate circuits employing memristors in Cadence Spectre. We report the phenomenological models of two different memristors we fabricated, the adjustment of a model developed by another group to match the behavior of our own device, the resulting Verilog-A model of our device, and finally utilization of this model in Cadence Virtuoso simulations of HCO circuits employing our memristors. Phase Portraits of the HCO circuit employing Pt electrode memristors show that through using memristors, it is possible to adjust oscillation rhythm and amplitude improving stable oscillation.

It has been encouraging to see that the model results are consistent and can be used in-circuit. Also contributing to memristor modelling and in-circuit using for this emerging research field is important for us. In our future works, we aim to fabricate the HCO circuit with our memristors and take measurements.

Acknowledgment

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