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24 April 2024

Thermal Performances of an Improved Package for Cryocooled Josephson Standards

Paolo Durandetto, Eugenio Monticone, Danilo Serazio, and Andrea Sosso

***Abstract*—Complex cryogenics still represents a strong limitation to the spread of Josephson voltage standards and cryogen-free cooling is particularly suitable to simplify their operation. The main downsides of liquid helium-free systems are related to the chip thermalization: indeed, at low temperature the heat transfer between the chip and the coldplate of a cryocooler in vacuum is strongly affected by the quality of the interfaces. In order to increase the thermal performances of cryocooled programmable Josephson standards we devised and tested a special cryopackage: the chip is embedded into a sandwich structure with high thermal conductivity materials subject to a controlled mechanical pressure to reduce thermal contact resistances. A thin sapphire lamina placed upon the chip allows the heat to be dissipated from the top, thus creating an additional path for the thermal flow. A special bridge-like system with a screw is used as reproducible torque-to-force converter to exert known pressures to the sandwich. Furthermore, we analyzed the effect of thermal contraction to the actual pressure exerted on the chip, showing a non-negligible increase when cooled down to cryogenic temperature that can be calculated and corrected for.**

***Index Terms*—programmable Josephson arrays, He-free refrigeration, heat transmission, thermal resistance, cryocooler**

I. Introduction

Several decades after the discovery of the Josephson effect [1], voltage standards based on this quantum phenomenon still represent one of the most complex and successful achievement of superconducting electronics. Hysteretic Superconductor-Insulator-Superconductor (SIS) technology has proved successful to fabricate arrays with tens of thousands Josephson junctions generating up to $10\,\mathrm{V}$ which enabled primary dc voltage calibrations to attain relative uncertainties as low as 10^{-11}[2]. Presently, quantum voltage standard research is focused on the application of Josephson arrays to ac and arbitrary signals: programmable Josephson voltage standards (PJVS) represent, so far, the most widely adopted technology to rapidly control the output voltage [3]. They use bias currents to activate/deactivate different segments with series connected junctions whose number follows a binary law, as in digital-to-analog converters of semiconductor electronics.

Refrigeration of Josephson voltage standards is generally achieved with liquid helium: this limits the spread of these quantum devices outside National Metrology Institutes, due to the increasing cost of liquid helium, driven by shortages rumors, and to the specific skills required for handling the potentially hazardous cryogen. Moreover, the difficulty of fabricating large and uniform arrays with high critical temperature superconductors, as YBCO and the more recent MgB_2 [4], still prevents the development of reliable Josephson standards working at higher temperatures.

Owing to the simpler operation, cryocoolers capable of reaching temperatures below $4\,\mathrm{K}$ bear a particular interest for Josephson standards, although several problems arise. The most relevant are related to thermal issues: the reduced cooling power and the high-vacuum environment of cryocoolers have important consequences on the behavior of devices, the more if a significant power is dissipated during the experiment. When a Josephson array is operated, it warms up because of the received rf and dc bias currents, raising local temperature and worsening the array operating margins. In such case, dissipating the electrical power while keeping the chip temperature suitably low is a challenge that adds to the typical problems in cryogen-free experiments.

Due to the low bias currents, the power dissipated into conventional SIS arrays is negligible and cryocooler integration was already demonstrated years ago [5]. This is not the case of non-hysteretic Josephson standards generating voltages varying with time, whose bias currents are in the mA range. Owing to the high output voltage obtainable and the number of bias lines, thermal issues in such arrays are the most challenging. Nevertheless, the cryocooler cooling power, that can exceed $1\,\mathrm{W}$ at $4.2\,\mathrm{K}$ in nowadays commercial closed-cycle refrigerators, is no longer the constraining factor. The main issue is rather the capability of the thermal links from the chip (typically fabricated on a silicon substrate) to the cryocooler cold surface to dissipate the electrical power, with a limited increase in chip temperature.

At low temperature, heat transfer between metals and dielectrics as Cu/Si strongly depends on the quality of the interfaces. For perfectly flat surfaces, thermal boundary resistance represents the unique limitation to the heat flux [6], whereas, in the case of significantly rough surfaces, the actual contact area is reduced and heat transfer is further limited by a bottleneck effect. It is known that the soldering of solid-solid joints represents the best solution to maximize the heat transfer at cryogenic temperature [7], since the melted solder fills very well the empty spaces between the solid surfaces. However, there are some drawbacks to this approach, as the possible degradation of the chip during the soldering, voids in the solder with reduced heat transfer [8] and failure due to repeated temperature cycling of the solder [9]. As alternative, the improvement of thermal contact conductance can be achieved both by applying a suitable mechanical pressure between chip and carrier and by interposing at their interface a soft material as indium, silver, tin or lead, which exhibits high thermal con-

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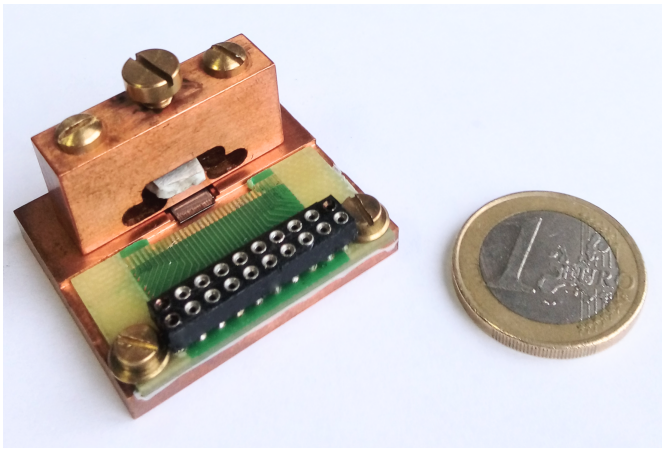
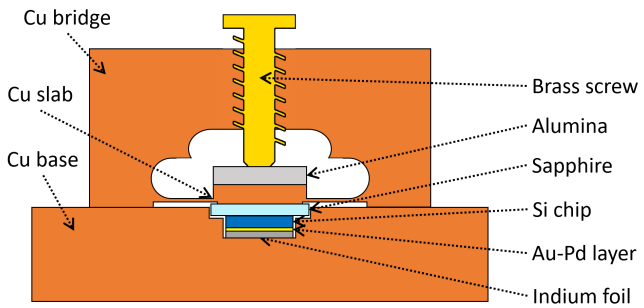


(a)



(b)

Fig. 1: (a) Special cryopackage for improved thermal dissipation and (b) its vertical front-view section (not in scale). Screw diameter and thread pitch are $4\,\mathrm{mm}$ and $0.7\,\mathrm{mm}$, respectively.

ductivity and low microhardness [10]. Mechanical pressure is a parameter that strongly affects the heat transfer between solid surfaces [11], [12] and should be controlled to obtain a good experimental reproducibility. Indium is usually preferred as thermal interface material in cryogenic applications [13], [14] as it remains soft and ductile at low temperature compensating differential thermal expansion between layers during thermal cycling.

In this paper we present and analyze a new cryopackage design for enhancing the thermal dissipation of a PJVS chip operated in the vacuum environment of a cryocooler. Its thermal resistance has been evaluated in different operating conditions by using some PJVS segments as a known heat-source, while other segments were used as temperature sensor by measuring their critical current. Study of heat transfer dependence on the applied mechanical pressure and on temperature was carried out and is described here.

II. System setup

A. Cryopackage

The Josephson chip is enclosed in the specially-designed cryopackage shown in Fig. 1a. Its schematic cross-section is also shown in Fig. 1b, where the overall sandwich shape is clearly illustrated. The chip is fabricated on a $0.5\,\mathrm{mm}$ thick Si substrate, fitted inside a groove into an oxygen-free high thermal conductivity (OFHC) copper block and suitably pressed against it by a bridge-like structure designed ad-hoc, whose section is similar to an arch closed at the bottom. A brass screw at the center of the bridge allows to press the chip against the sample holder by means of a thin Cu bottom slab, made flexible by appropriate slots. At the same time, the slab provides good thermal link to the holder. A $0.1\,\mathrm{mm}$ thick Heat-Spring® indium foil[1] [15] was placed between the Cu base and the chip. Furthermore, to provide a clean interface, indium oxide was mechanically removed from the In foil surface. For the same reason, the chip backside was sputter cleaned and covered by a AuPd layer of $400\,\mathrm{nm}$. The upper side of the chip is electrically insulated from the Cu slab of the pressing bridge by a $0.3\,\mathrm{mm}$ thick c-plane sapphire lamina, which provides an additional via for heat transmission because of its low thermal resistivity. A thin Apiezon N layer was applied to both chip-sapphire and bridge-sapphire interfaces to further increase heat transfer.

All these layers are then pressed against the base-holder by means of the aforementioned bridge-screw system. Its operation is straightforward: a calibrated torque screwdriver is used to turn the central screw and, hence, to produce a pressing force. The relation between torque and force has been previously measured by means of a home-built calibrated load-cell positioned just under the flexible slab, in place of the Cu base-chip structure. In this way, the torque-to-force calibration curve of the pressing bridge was obtained, which was then used in the measurements with the Josephson chip. As shown in Fig. 1, the screw acts on an alumina spacer that in turn transfers the applied force to the flexible slab. The alumina spacer is used to avoid the wear of the slab as a result of the strong contact with the brass screw.

The torque-to-force relation is almost linear in the interval of our interest, whose upper force of $500\,\mathrm{N}$ results from an applied torque of $0.2\,\mathrm{N\,m}$ and limits the deformation of the pressing bridge in the normal direction ($< 10\,\mu\mathrm{m}$).

B. Josephson chip

The PJVS chip used in this experiment was fabricated in cooperation with PTB (Physikalisch-Technische Bundesanstalt) with the Superconductor-Normal-Insulator-Superconductor (SNIS) technology [16], developed for applications in quantum voltage metrology and with peculiar characteristic in terms of reduced temperature dependence of the electrical parameters [17]. Its operation was intensively investigated both in liquid helium and in cryocooler [18], [19]. It is made by 8192 series-connected Nb/Al-AlO_x/Nb junctions, which are sub-divided into fourteen individually-biased binary segments. This feature of PJVS arrays has been exploited in this work by using some segments as power source and others as temperature sensor, using the procedure explained in Sec. III and previously adopted in [20] and [21].

[1]Brand names are used for identification purposes. Such use implies neither endorsement by INRiM nor assurance that the equipment is the best available.

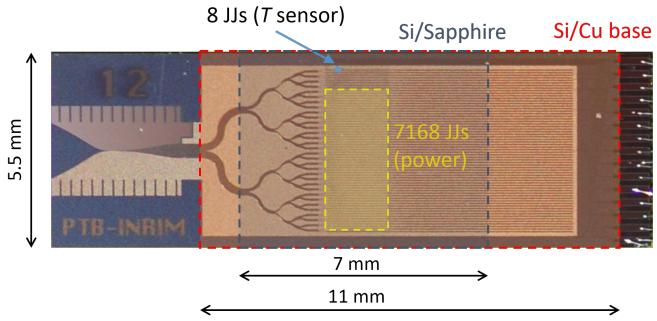


Fig. 2: 1 V SNIS PJVS array with 8192 junctions. Up to 7168 junctions (3 segments, yellow dashed line) were used to generate electrical power. A single segment made up by 8 junctions was used as temperature sensing element. The red dashed line indicates the area of the chip backside in contact with the Cu base (with In and AuPd as interfaces). The blue dashed line indicates the area of the chip upper side in contact with the sapphire lamina (Apiezon N as interface).

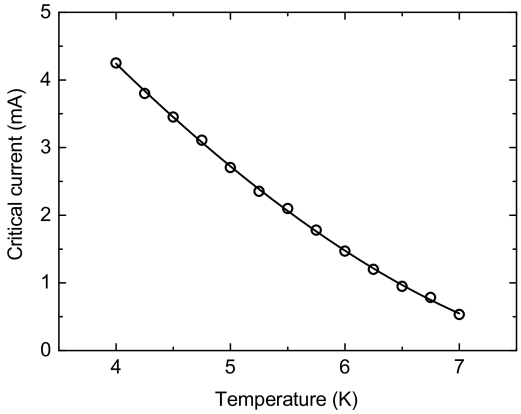


Fig. 3: Critical current vs. temperature of the 8 junctions sub-array employed as temperature sensor. The experimental points are fitted with a power function. More details are given in the text.

C. Cryogenic apparatus and measurement instruments

The employed cooling system is based on a two-stage Gifford-McMahon cryocooler[2] with a minimum temperature near 2.9 K (no thermal load) and nominal cooling power of 1 W at 4.2 K. The cryocooler cold finger is fitted with an additional copper disk, the coldplate, upon which the cryopackage base is properly tightened. A thin layer of Apiezon N is applied at this Cu/Cu interface. The coldplate hosts a silicon diode thermometer and a heater wire wound around it, allowing temperature monitoring and control. A second Si thermometer, placed directly on the Cu bridge and close to the chip, is used to detect possible thermal gradients related to PJVS power dissipation.

Critical currents were evaluated from observed current to voltage dependence of array sections, obtained with a high-accuracy current source and a digital voltmeter. Additional current source and voltmeter were devoted to generate and accurately measure the electrical power dissipated in the heating junctions.

III. Measurement of Temperature Variations

To investigate the thermal behavior of our cryopackage, i.e. to evaluate its thermal resistance $R = \Delta T/P$, some of the sub-arrays within the PJVS (Fig. 2), counting 7168 junctions, were chosen as elements to generate a known amount of electrical power P by biasing them at currents higher than the critical current value. A single segment with 8 junctions was instead used to sense the power-induced temperature variation ΔT, based on the dependence of critical current on junctions temperature. In both cases we used a 4-wire configuration, that allowed to accurately estimate the generated electrical power and measure the critical current I_c of the temperature sensing junctions. To determine the chip temperature from I_c measurements, the $I_c(T)$ dependence of the sensing sub-array was measured first over the relevant range in cryocooler and without extra power from the heating segments. A dc current was fed through the heater wire to vary the coldplate temperature, that was measured with a calibrated sensor after it reached a stable point, i.e. after few cryocooler time constants [22]. Chip temperature was estimated to be the same as the coldplate, since very low heat is generated during I_c measurements and the gradient across its thermal resistance path to the coldplate is then negligible. The $I_c(T)$ experimental data points are shown in Fig. 3: they are well fitted by the power equation $I_c(T) = I_0\,(1 - T/T_c)^a$, with $I_0 = 12.6\,\mathrm{mA}$, $T_c = 8.18\,\mathrm{K}$ and $a = 1.62$. This equation has then been used for chip temperature determinations. I_c was checked before and verified at the end of all measurements.

[2]Leybold 4.2 GM.

IV. Results

A. Dependence on the mechanical pressure

As previously described in Sec. II-A, we employed the bridge-screw system to exert reproducible normal forces for pressing the chip against the Cu carrier and determine the relationship with the package thermal resistance. The experimental trend of the overall thermal resistance vs. the applied pressure on the Si/In/Cu contact surface ($5.5\,\mathrm{mm} \times 11\,\mathrm{mm} = 60.5\,\mathrm{mm}^2$, see Fig. 2) at different temperatures is shown in Fig. 4. As expected, both mechanical pressure and operating temperature affect the thermal resistance of the cryopackage, that decreases with the pressure following roughly a linear behavior.

In [11], Howe *et al.*, using a pressed indium foil as thermal interface material between a 10 V PJVS chip and the Cu carrier, measured $R \simeq 1.6\,\mathrm{K\,W^{-1}}$ at 3.2 MPa and 4 K, with a contact area $A \simeq 2\,\mathrm{cm}^2$. To normalize R with respect to the Si/In/Cu contact surface, we evaluate the $R \cdot A$ product, a parameter independent on A. In our case, $R \cdot A = 1.9\,\mathrm{K\,W^{-1}} \cdot 0.605\,\mathrm{cm}^2 = 1.1\,\mathrm{K\,cm^2\,W^{-1}}$ at 4 K and 3.2 MPa, whereas the package presented in [11] gives $R \cdot A = 3.2\,\mathrm{K\,cm^2\,W^{-1}}$. The lower $R \cdot A$ value obtained with our cryopackage is likely due

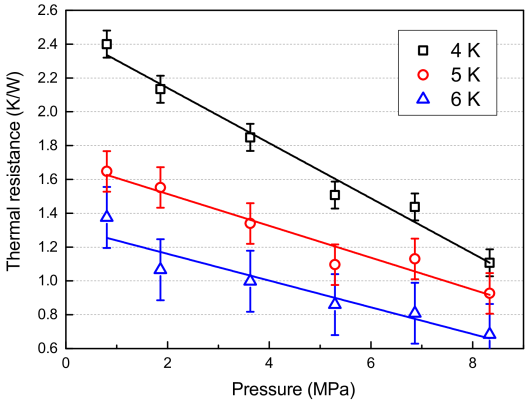


Fig. 4: Cryopackage thermal resistance vs. applied mechanical pressure at different temperatures of the coldplate.

to the additional upward conduction through the sapphire layer and to the particular indium foil employed.

Due to the multilayered structure, the overall thermal resistance is the sum of resistances of bulk layers and interfaces between them. The thermal resistance of the thick layers in the structure can be evaluated by the simple heat transfer equation $R = (k\,S/d)^{-1}$, where k is the thermal conductivity, d the layer thickness and S the layer surface. Assuming $S = 5.5\,\mathrm{mm} \times 7\,\mathrm{mm} = 38.5\,\mathrm{mm}^2$ for every layer, given by the smaller contact surface in the sandwich, a worst case is studied. At $4\,\mathrm{K}$ we have estimated $R \simeq 0.13\,\mathrm{K\,W^{-1}}$ for the chip ($k \simeq 1\,\mathrm{W\,K^{-1}\,cm^{-1}}$ for our Si substrate [23] and $d = 0.5\,\mathrm{mm}$), and $R \simeq 0.078\,\mathrm{K\,W^{-1}}$ for sapphire ($k \simeq 1\,\mathrm{W\,K^{-1}\,cm^{-1}}$ [24] and $d = 0.3\,\mathrm{mm}$). For Heat-Spring® indium the thermal conductivity has been obtained using the Wiedemann-Franz law, where electrical resistivity has been measured at $4\,\mathrm{K}$. With $k \simeq 6\,\mathrm{W\,K^{-1}\,cm^{-1}}$ and $d = 0.1\,\mathrm{mm}$ the thermal resistance for In is $R \simeq 0.004\,\mathrm{K\,W^{-1}}$. A significant contribution could derive from the thin layers of Apiezon N at the Si-sapphire and Cu-sapphire interfaces. The thickness of the layers was estimated applying an increasing pressure between 0.5 and $6\,\mathrm{MPa}$ on Apiezon N flattened between two sapphire laminae. For pressures higher than $1\,\mathrm{MPa}$ the thickness was less than $1\,\mu\mathrm{m}$, from which, with a thermal conductivity of $k \simeq 0.004\,\mathrm{W\,K^{-1}\,cm^{-1}}$ [25], a thermal resistance of about $R \simeq 0.065\,\mathrm{K\,W^{-1}}$ is found. The thermal resistance of the AuPd layer is assumed to be negligible. The sum of these single-layer values of R is about $0.34\,\mathrm{K\,W^{-1}}$ and is quite low compared to the experimental results in Fig. 4, clearly indicating that, as expected, the main contribution to the cryopackage thermal resistance derives from the interfaces.

B. Effect of the additional top conduction

In this section we want to assess the effectiveness of the sapphire lamina placed on the top of the chip as an additional heat-flow path. To this aim, we replaced it with a fused-silica glass substrate of the same thickness ($0.3\,\mathrm{mm}$). Fused-silica thermal conductivity is around four orders of magnitude lower

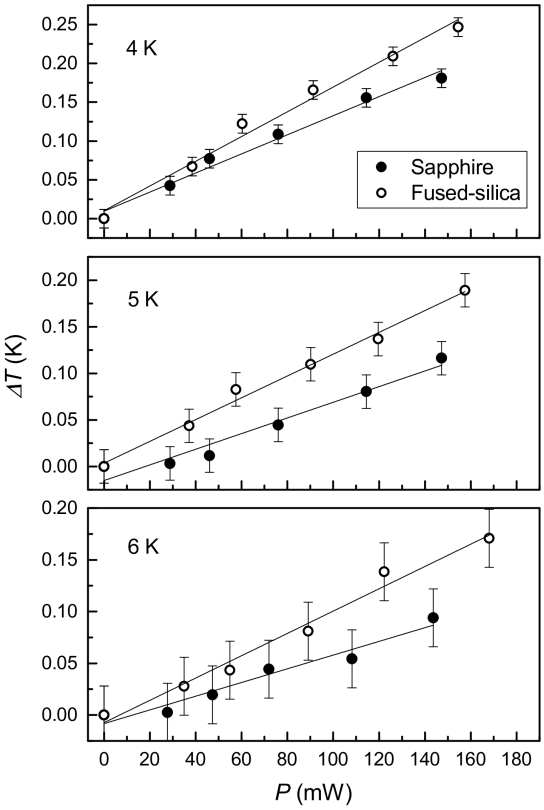


Fig. 5: Temperature increase ΔT caused by the dissipated power P with sapphire (closed circle, enabled top conduction) and fused-silica glass (open circle, disabled top conduction) placed over the chip. Data were taken at different temperatures of the coldplate and with a mechanical pressure of $8.3\,\mathrm{MPa}$.

than sapphire one [24], thus, it acts as a high resistance for the upward heat current.

This test has been performed with an exerted mechanical pressure of about $8.3\,\mathrm{MPa}$, which corresponds to the upper limit of the forces employed in the previous experiment (Sec. IV-A). It is important to note that the indium foil, once pressed above its yield stress ($\sim 2.1\,\mathrm{MPa}$), does not recover its original shape and its reliability is guaranteed only when the applied pressure is further increased. Therefore, in order to avoid systematic errors due to the non optimal contact between the chip and indium, the latter was replaced with a new one in this second experiment. In Fig. 5 the temperature increase is plotted as a function of the applied electrical power in the two cases of enabled (sapphire) and disabled (fused-silica) top conduction and at different coldplate temperatures.

The cryopackage thermal system can be modeled by its analogue electrical circuit, where two resistances R_t and R_b, representing respectively the top and the bottom paths, are connected in parallel. The equivalent resistance of such circuit R_{tb} is the one measured in Sec. IV-A with the sapphire lamina on the upper face of the chip. Replacing sapphire with glass allows to determine the single bottom resistance R_b, since top conduction is prevented by the high thermal

TABLE I: Cryopackage thermal resistance contributions at 8.3 MPa at different temperatures of the coldplate.

T (K)	R_{tb} (K W^{-1})	R_b (K W^{-1})	R_t (K W^{-1})	$\frac{R_b}{R_{tb}}$
4	1.23	1.59	5.43	1.29
5	0.84	1.17	2.98	1.39
6	0.66	1.08	1.70	1.64

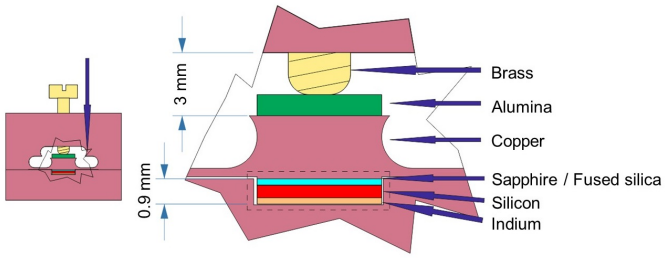


Fig. 6: Particular of the cryopackage elements that may contribute to a pressure change between 300 K and 4 K.

resistivity of fused-silica. Hence, the thermal resistance of the additional heat conducting path can be evaluated by $R_t = R_{tb}\,R_b/(R_b - R_{tb})$. The results are summarized in Tab. I and confirm that a substantial contribution to the overall heat transfer is provided by the enabled top conduction, which increases heat transmission by lowering the cryopackage thermal resistance by 30 % at 4 K up to 60 % at 6 K. Since thermal resistances are dominated by interfaces, this means that, at higher temperatures, chip-sapphire and sapphire-Cu interfaces become more performing than those in the bottom path.

C. Estimation of the actual pressure at low temperature

As previously described, the chip is installed and pressed in the sample holder at room temperature and subsequently cooled down to 4 K. Therefore, thermal contraction or expansion of the cryopackage components may cause the actual pressure to change with respect to the one applied before the cooling. A rough estimation of this effect can be obtained by using the thermal contraction coefficients to calculate the variations in height of each element of the cryopackage. Observing the scheme in Fig. 6 it is easy to understand that the whole Cu body may contribute to a pressure change only for 3.9 mm of its height, that is the part shared with the inner elements of the package. Hence, the difference δ between the thickness change of this relevant Cu part and that of the inner components was evaluated ($\delta = \Delta_{\text{Cu}} - \sum_{\text{in}} \Delta_{\text{in}}$). Due to its very low thickness, the contribution of the AuPd layer is neglected in this evaluation.

Tab. II shows the variations Δ between 300 K and 4 K for each element according to the thermal expansion coefficients found in the literature [26], [27], [28], [29]. The calculated variation differences are $\delta \simeq 3.5\,\mu$m and $\delta \simeq 3.7\,\mu$m, respectively with the sapphire and the fused silica laminae placed over the Si chip. In both cases δ is positive, meaning that the relevant Cu part shrinks more than the internal components, which in turn leads to an increased pressure when the package is cooled.

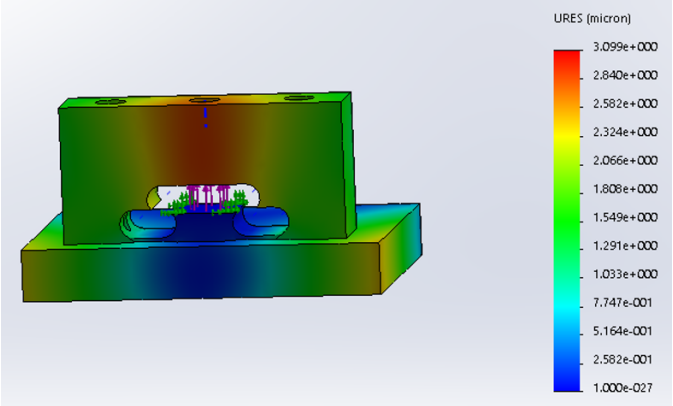


Fig. 7: Simulated cryopackage deformation due to an upward force of 200 N (purple arrows). More details are given in the text.

The increase of mechanical pressure has been evaluated both experimentally and through simulation, assuming that is related to the deformation δ of the top of the pressing bridge in the normal direction. Using a dial gauge, we measured the relation between vertical deformation and exerted normal force at room temperature: an approximately linear trend has been obtained, from which follows that forces around 175 N and 185 N are respectively required to flex the bridge by 3.5 µm and 3.7 µm, corresponding to mechanical pressures of 2.9 MPa and 3.1 MPa. In order to validate these experimental findings, a SolidWorks static analysis of the cryopackage elastic deformation has been performed. In this model, the actual conditions are simplified as possible: the entire cryopackage is considered as a unique copper body and disjointed from the cryocooler coldplate. The effect of thermal contraction is simulated with an upward normal force exerting on the bridge, which then causes its deformation. As shown in Fig. 7, it has been found that a force of 200 N is required to flex the top of the bridge of about 3 µm, consistent with the experimental analysis.

Both tests entail that all the measurements presented in the previous sections should be corrected by adding an offset of about 3 MPa to evaluate pressure values around 4 K from that measured at room temperature. Thus, for example, the corrected x-axis range of Fig. 4 should be approximately $4 \div 11$ MPa. From such corrected graph it is possible to derive the thermal resistance dependence on the actual pressure at low temperature, independent of the mechanical properties of the cryopackage. As regards the comparison in Sec. IV-B, since the δ value in the disabled-top conduction scenario (3.7 µm) is slightly larger with respect to the enabled one (3.5 µm), the actual pressure at low temperature turns to be higher as well. However, this difference can be neglected and, if not, it would underestimate the thermal resistances R_b and the performance improvement factors R_b/R_{tb} listed in Tab. I, thus confirming our worst-case analysis.

TABLE II: Thickness variation of each cryopackage element that may contribute to a pressure change between $300\,\mathrm{K}$ and $4\,\mathrm{K}$. See description in the text.

Element	Thickness at $300\,\mathrm{K}$ (mm) $d_{300\mathrm{K}}$	Thermal contraction coefficient (%) $\frac{d_{300\mathrm{K}}-d_{4\mathrm{K}}}{d_{300\mathrm{K}}}$	Variation at $4\,\mathrm{K}$ (µm) $\Delta = d_{300\mathrm{K}} - d_{4\mathrm{K}}$
Cu (base + bridge)	0.9 + 3 = 3.9	0.326	12.71
Brass screw	2	0.384	7.68
Alumina	1	0.064	0.64
Sapphire (or fused silica glass)	0.3	0.061 (-0.008)	0.183 (-0.024)
Si chip	0.5	0.022	0.11
In foil	0.1	0.64	0.64

V. Conclusion

A special cryopackage suitable for the cryogen-free operation of programmable Josephson standards around liquid helium temperature has been designed and tested. It exploits low-temperature properties of materials, like indium and sapphire, with a sandwich-structure that noticeably enhances the dissipation of the electric power generated inside the device. A special pressing bridge-like system made of copper was designed and calibrated at room temperature to apply a known normal force to the sandwich as a way to control the thermal contact resistances of the interfaces, which are shown to be the limiting factor, assuring that the operating conditions of thermal measurement are reproducible. The actual mechanical pressure exerted at cryogenic temperature has been approximately estimated from the cryopackage thermal contraction, resulting in a non-negligible increase with respect to the one applied at room temperature.

Although our investigation was based on a $1\,\mathrm{V}$ PJVS, this cryopackage can be even more effective for the $10\,\mathrm{V}$ PJVS, that has a larger contact surface with powers up to $350\,\mathrm{mW}$ to be transferred to the coldplate.

Acknowledgment

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