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Improvements on electronic technology in recent years have allowed the application of digital techniques in phase noise metrology, where low noise and high accuracy are required, yielding flexibility in system implementation and setup. This results in measurement systems with extended capabilities, additional functionalities, and ease of use. In most digital schemes, the Analog to Digital Converters (ADCs) set the ultimate performance of the system; therefore the proper selection of this component is a critical issue. Currently, the information available in the literature describes in depth the ADC features only at frequency offsets far from the carrier. However, the performance close to the carrier is a more important concern. As a consequence, the ADC noise is, in general, analyzed on the implemented phase measurement setup. We propose a noise model for ADCs and a method to estimate its parameters. The method retrieves the phase modulation and amplitude modulation noise by sampling around zero and maximum amplitude, a test sine-wave synchronous with the ADC clock. The model allows discriminating the ADC noise sources and obtaining the phase noise and amplitude noise power spectral densities from 10 Hz to one half of the sampling frequency. This approach reduces the data processing, allowing an efficient ADC evaluation in terms of hardware complexity and computational cost. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4984948]

I. INTRODUCTION

New methods for the phase and amplitude noise measurement of oscillators have been proposed in the past years based on digital systems.[1–8] Some reasons are just obvious: reconfiguration flexibility and compactness of digital hardware. Others are more subtle. The traditional method based on two mixers and cross spectrum[9–12] requires two oscillators at the same frequency of the oscillator under test, while in a fully digital implementation, arbitrary frequencies are synthesized numerically with a resolution exceeding any practical use ($\sim 6 \times 10^{-18}$ with 64 bits numerically controlled oscillator). Another reason is that the traditional scheme suffers from artifacts and errors.[13,14] Similar artifacts and errors, if any, have still not been made clear in the case of digital systems.

The increasing technological advances on Analog to Digital Converters (ADCs), in terms of resolution and sample rate, have allowed the implementation of phase/amplitude noise metrology as ideal Software Defined Radio (SDR) states,[15] sampling the signal of interest through a high-speed ADC and processing the data digitally, reducing at minimum the analog components. However, the progress in digital measurement of amplitude and phase noise has been rather slow for a number of reasons. First, the availability of converters with sufficient resolution and speed, i.e., converters with features such as 14–16 bits and sampling rates higher than 100 Mega Samples per second (MSps), is rather recent. Second, the skill for digital hardware design and for Radio Frequency (RF) engineering, oscillators, spectral purity, etc., is seldom found in the same team. Third, the measurement of amplitude and phase spectra relies on some generally undocumented features of the converters.

This article focuses on a model of the ADC, specific for the measurement of oscillators, and on a method to extract the parameters. We work on a Red Pitaya board because this platform is suitable for our tests with acceptable experimental complexity. Resolution and speed (14 bits, 125 MSps) are reasonably close to the state of the art of ADCs (16 bits, 350 MSps or 14 bits, 1 GSps), and it is potentially sufficient for the implementation of a complete instrument. Of course, a similar test with cutting edge converters will follow.

Different techniques have been developed for characterizing ADCs. While the histogram approach has been widely used for measuring static errors,[16,17] one group[18] proposed a method for estimating the voltage error generated by the aperture jitter plus the internal additive noise through the locked histogram technique, performing synchronous sampling. The distribution function of the noise, assumed normal, was obtained by modifying the mean of the input sine-wave by adjusting an offset as finely as one least significant bit (LSB) of the ADC under test, being a suitable approach for ADCs of low/medium resolution (maximum 10 bits). Other work[19] proposed a model for the jitter of ADCs and a method based on signal-to-noise ratio (SNR) analysis in order to evaluate and discriminate the effects of the jitter components on the ADC performance, thereby giving a guideline to compensate

for such effects in future high-speed ADC designs. A characterization technique based on the use of a Graychip and down-conversion was performed[1] for evaluating the viability and strategies of the direct-digital technique implementation for phase noise measurements. Characterization of high resolution, low speed ADCs (≥20 bits, ≤5 MHz) have been performed[20] using a Programmable Josephson Voltage Standard. Recent results of high-speed ADC noise characterization were obtained through a full digital approach based on common noise cancellation and digital down-conversion.[21] The power spectra density of ADC phase noise is estimated after proper filtering and decimation stages.

In view of the fast advances in technology for obtaining high speed and high resolution ADCs and in the frame of evaluating ADCs for phase/amplitude noise metrology applications, this work proposes a computational low cost method for ADC noise characterization using a commercial system setup. We present a model for ADC noise and measurement for determining their components through Phase Modulation (PM) and Amplitude Modulation (AM) analysis, tracking the relevant information by synchronous sampling. The results of the characterization will provide information about the limit for phase/amplitude noise metrology allowing punctual consideration in measurement techniques design.

II. ADC NOISE MODEL

The model proposed in this work aims to discriminate the different noise contributions of analog to digital conversion in the basis of two random noise classes: additive and parametric.[22] Additive noise refers to a noise process that can be represented as a voltage or a current added to the signal, caused by the thermal noise on resistive elements and by shot and avalanche noise present in the junctions of semiconductors.[23] This noise is generated in the signal bandwidth and it is always present, even without carrier information. Instead, parametric noise refers to a non-linear near-DC process caused by non-linearities present in electronic circuits due to contamination in semiconductors materials.[23] It is translated by action of a carrier, generating amplitude and/or phase modulation on the signal.

Our ADC noise modeling focuses on four main noise sources, as it is depicted in Fig. 1(a): input stage, aperture jitter, voltage reference, and quantization.

The contribution of the noise generated by the input stage has two components: additive and parametric. For the model proposed here, this noise source is assumed to be dominated by the additive noise $n(t)$. This assumption is verified through the experimental results reported in Sec. IV. Hence, considering an input signal $v(t)$, the effect of the input stage noise is expressed as $v'(t) = v(t) + n(t)$.

The aperture jitter, $\mathsf{x}(t)$, defined as the variation of the sampling instant kT_s, is caused by time fluctuations in the sample and hold.[24,25] These time fluctuations generate a parametric noise whose effects over the sampled signal are described by $v''_k = v'(kT_s + \mathsf{x}_k)$, where $\mathsf{x}_k = \mathsf{x}(kT_s)$.

At this point, the sample v''_k is converted into a digital value, as described in (1), where m is the resolution of the ADC, V_r is the voltage reference, and n_q is the quantization noise,

$$\hat{v}_k = v''_k \frac{2^m}{V_r} + n_q. \tag{1}$$

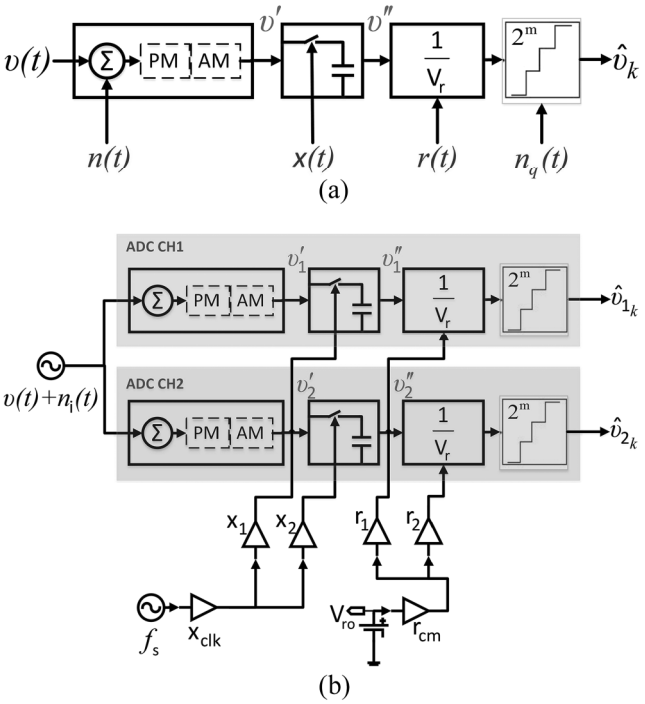

FIG. 1. (a) ADC noise modeling. The parameters of the model represent the four noise sources involved in an acquisition process: input stage circuit, aperture jitter, voltage reference, and quantization. (b) Key interplay in dual converters. Discrimination between common noise and single channel noise sources in dual converters.

The voltage reference is considered as a non-ideal source, $V_r = V_{r_0}(1 + r(t))$, represented by the nominal value V_{r_0} and the relative noise $r(t)$. This noise source is presented as a parametric noise whose features depend on the voltage reference typology.[26]

The quantization noise n_q, well described currently in the literature,[27] generates white phase noise spread along the Nyquist bandwidth ($\frac{1}{2T_s}$). For high resolution ADCs, like the one studied here, the effective number of bits (ENOB) is significantly lower than the nominal value; therefore, the effect of this noise source can be neglected, at first order, with respect to the other noise contributions and for this reason it is not included in the model proposed.

Considering m and V_{r_0} constant values and in analogy with operational amplifiers, it is convenient to refer the noise at the input by dividing the output by $\frac{2^m}{V_{r_0}}$. Then, the ADC output referred at the input can be expressed as $\tilde{v}_k = \hat{v}_k \frac{V_{r_0}}{2^m}$.

Under the assumption of $r << 1$, the ADC output is described by (2), where $n_k = n(kT_s)$, $\mathsf{x}_k = \mathsf{x}(kT_s)$, and $r_k = r(kT_s)$ are discrete-time random processes obtained from sampling the corresponding continuous-time random process at $t = kT_s$,

$$\tilde{v}_k = (n_k + v(kT_s + \mathsf{x}_k))(1 - r_k). \tag{2}$$

Now that the ADC output is stated in terms of the noise sources, we can analyze their effects using a proper input for

discriminating their contributions. Following (2), the contribution of x_k propagates to the ADC output depending on the slew rate of the input signal, while the impact of r_k depends on the input signal level. Note that in the case of $v(t) = 0$, the contribution of the aperture jitter and the voltage reference noise are negligible; therefore, the ADC output corresponds to the additive noise of the input stage.

Then, assuming $v(t) = V_0 \cos(2\pi\nu_0 t)$ as input signal of the ADC, case of interest for time and frequency applications, we can rewrite (2) as

$$\tilde{v}_k = (n_k + V_0 \cos(2\pi\nu_0(kT_s + \mathsf{x}_k)))(1 - r_k). \tag{3}$$

Considering n_k, x_k, and r_k independent processes, the total amplitude and phase noise generated by the ADC can be expressed as the sum of the different amplitude and phase fluctuations induced by each noise source, respectively. The additive noise of the input stage n_k generates amplitude and phase noise on the signal converted. In order to better discriminate its effects, this noise source is decomposed in its in-phase and quadrature components, n_α and n_φ, respectively. Under low noise conditions,[22] $|n_\alpha/V_0| \ll 1$ and $|n_\varphi/V_0| \ll 1$, the normalized amplitude noise generated by n_k is expressed as $\alpha_{n_\alpha} = (1/V_0)n_\alpha$, while the induced phase noise is given by $\varphi_{n_\varphi} = (1/V_0)n_\varphi$.

The aperture jitter x_k results in pure phase modulation on the analog to digital conversion given by $\varphi_\mathsf{x} = 2\pi\nu_0\mathsf{x}$. The maximum voltage variations induced by this noise source occur at the samples of highest slew rate (SR), i.e., close to the zero-crossings and are described by $V_0 2\pi\nu_0\mathsf{x}_k$. Moreover, it is worth to remark that the samples of maximum amplitude are not influenced by this noise contribution at the first order. Instead, they are directly related to the voltage reference noise presented as amplitude modulation on the signal converted. It generates a maximum voltage error $V_0 r_k$ that occurs at the maximum amplitude samples of the input signal.

Hence, the total ADC phase noise φ_k and the total ADC amplitude noise α_k are described in (4), where φ_k is in radians and α_k is non-dimensional, being the normalized amplitude fluctuations,[22]

$$\begin{aligned}\varphi_k &= \varphi_{n_{\varphi_k}} + \varphi_{\mathsf{x}_k} = \frac{1}{V_0} n_{\varphi_k} + 2\pi\nu_0\mathsf{x}_k,\\ \alpha_k &= \alpha_{n_{\alpha_k}} + r_k = \frac{1}{V_0} n_{\alpha_k} + r_k.\end{aligned} \tag{4}$$

Since power spectral density (PSD) and polynomial law are considered meaningful tools for noise description and analysis due to the straightforward identification of the different noise processes,[22] they are used for representing the ADC noise contributions. Hence, the PSD of the ADC phase noise in rad^2/Hz and the PSD of the ADC amplitude noise in 1/Hz are described in (5), where the integer $N < 0$ depends on the device,

$$S_{\varphi,s}(f) = \sum_{j=N}^{0} \mathsf{b}_{s_j} f^j \qquad S_{\alpha,s}(f) = \sum_{j=N}^{0} \mathsf{h}_{s_j} f^j. \tag{5}$$

The difference between the analog bandwidth B and the sampling frequency f_s in a digital circuit generates aliasing on the white noise region of the sampled signal spectrum.[28] Hence, the voltage noise spectrum of the sampled signal can be represented as $S_{\tilde{v}}(f) = \frac{2B}{f_s}\mathsf{h}_0 + \sum_{j=N}^{-1} \mathsf{h}_j f^j$ (V^2/Hz). For the case of the aperture jitter, aliasing is generated in the white noise region of the spectrum, caused by the fact that these fluctuations are sampled at the sampling clock (f_s). Thus, the spectrum of x_k can be expressed as $S_{\mathsf{x},s}(f) = \frac{2}{f_s}\mathsf{J}^2 + \sum_{j=N}^{-1} \mathsf{k}_j f^j$ (s^2/Hz), where J is the root mean square (rms) time fluctuation of the aperture jitter and $\mathsf{k}_0 = \frac{2}{f_s}\mathsf{J}^2$. The spectrums of n_{φ_k}, n_{α_k} (V^2/Hz), and r_k (1/Hz) represented through the polynomial law are described in (6). Since r_k represents a relative amplitude noise, the coefficients h_{r_j} are non-dimensional,

$$\begin{aligned}S_{n_\varphi,s}(f) &= \sum_{j=N}^{0} \mathsf{h}_{\varphi_j} f^j \qquad (\text{V}^2/\text{Hz}),\\ S_{n_\alpha,s}(f) &= \sum_{j=N}^{0} \mathsf{h}_{\alpha_j} f^j \qquad (\text{V}^2/\text{Hz}),\\ S_{r,s}(f) &= \sum_{j=N}^{0} \mathsf{h}_{r_j} f^j \qquad (1/\text{Hz})\,.\end{aligned} \tag{6}$$

Hence, from (4), the spectrums of the phase and amplitude noise of the ADC are

$$\begin{aligned}S_{\varphi,s}(f) &= \frac{1}{V_0^2} S_{n_\varphi,s}(f) + 4\pi^2 {\nu_0}^2 S_{\mathsf{x},s}(f),\\ S_{\alpha,s}(f) &= \frac{1}{V_0^2} S_{n_\alpha,s}(f) + S_{r,s}(f).\end{aligned} \tag{7}$$

In this manner, from (7) the contribution of each noise source for each different noise process could be identified having a complete description of the device limitations.

III. METHOD FOR ADC NOISE CHARACTERIZATION

As second part of this work, we propose a method for determining the ADC noise components stated in the model. The method is based on data acquisitions under three different measurement conditions that allow characterizing the three main noise process of the model: input stage, aperture jitter, and voltage reference. In the first condition, the input of the ADC is connected to ground through a 50 Ω resistor. In this case, the contribution of $\mathsf{x}(t)$ and $r(t)$ is negligible since the slew rate and the level of the signal are zero. Therefore, the voltage noise on the data acquired is totally related to the additive noise of input stage. The other two measurements are made by sampling synchronously two points of the cosine-wave at the input: the zero-crossings and the peak values.

Considering that the voltage noise of the zero-crossings is directly related to phase fluctuations (PM), the measurement of these variations will result in the estimation of the phase noise generated by $n_\varphi(t)$ and $\mathsf{x}(t)$. On the other hand, the voltage noise on the peak values is representative of the amplitude fluctuations (AM); therefore, the measurement of the variation of these samples from period to period will yield the amplitude noise added by $n_\alpha(t)$ and $r(t)$. Hence, the total ADC noise can be estimated through these measures as described in (8), where $S_{\tilde{v},\varphi}$ and $S_{\tilde{v},\alpha}$ are the PSD of the voltage noise of the signal sampled at zero-crossings and at the peak values,

respectively,

$$S_{\varphi,s}(f) = \frac{1}{V_0^2} S_{\tilde{v},\varphi},$$
$$S_{\alpha,s}(f) = \frac{1}{V_0^2} S_{\tilde{v},\alpha}. \tag{8}$$

It is important to notice that with a single channel configuration, the noise obtained is also influenced by the noise contributions of the sampling clock and the input signal generator. Since the objective of this work is to characterize the ADC for phase noise metrology which, in general, is based on differential techniques, we propose a configuration with two independent channels as depicted in Fig. 1(b). The common noise contributions, such as the one coming from the input signal generator, the sampling clock, and the voltage reference, are canceled by subtracting the data obtained from the two channels. In consequence, the noise estimated is the contribution of the two ADC channels. Since the channels are assumed to be uncorrelated, the noise of a single channel is half the total noise.

The scheme of the synchronous sampling system, which is in charge of acquiring the zeros-crossings and the peaks of the cosine-wave, is shown in Fig. 2. The principle of operation consists in aligning the input signal to the sampling clock by means of a Phase Locked Loop (PLL): the input signal is sampled and sent to a Proportional-Integral controller (PI) which drives the frequency of the signal generator through a DAC, providing the proper phase information. The input signal generator works as a Voltage Controlled Oscillator (VCO) correcting the signal generated to acquire the selected point, either for AM or PM characterization. In closed-loop condition and under the configuration for PM characterization (acquisition of zero-crossings), it is possible to sample an input signal whose frequency is multiple of the sampling clock by means of sub-sampling. To extend the measurements at lower frequencies (ν_0 sub-multiple of f_{clk}) the data rate is down-sampled. Therefore, the sampling frequency f_s becomes equal to the input frequency ν_0, ($f_s = \frac{f_{clk}}{M} = \nu_0$). For AM characterization, we provide an input frequency not higher than quarter the sampling clock in order to guarantee the peaks acquisition. In this case, the system is still synchronized through the zero-crossings but only the peak values are acquired.

The PSD of the ADC noise is estimated in a bandwidth equal to the Nyquist frequency. The corresponding information

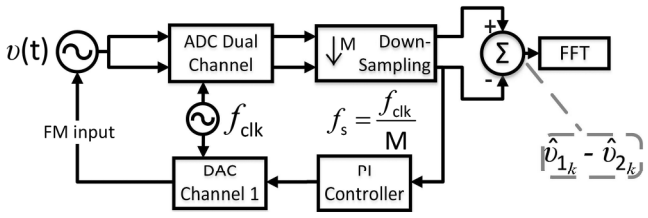

FIG. 2. The scheme proposed allows sampling synchronously one sample per period in order to measure, through its variations, the ADC noise effect on the output, as amplitude and phase fluctuations. The implementation is based on a dual ADC and through the difference of the two outputs, the common noise is canceled obtaining only the corresponding noise contribution of each channel.

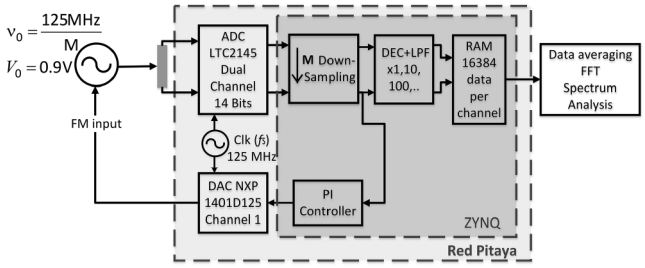

FIG. 3. Block diagram of method implemented in Red Pitaya platform. The data processing is performed offline using approximately 2×10^9 samples per each ADC channel.

at low frequencies is obtained through six stages of decimation in order to acquire data down to 10 Hz or less according to the sampling frequency. Blocks of 16384 data per channel are post-processed offline using MATLAB.

Figure 3 depicts a simplified block diagram of the method implemented in the Red Pitaya platform.[29] The latter is an open source embedded system that includes a dual-channel 14 bits ADC at 125 MSps LTC2145 from Linear Technology, a dual-channel 14 bits DAC at 125 MSps DAC1401D125 from NXP Semiconductors, and a Zynq 7010 System On Chip (SoC) from Xilinx. The input stage of Red Pitaya was modified by bypassing the amplifier and the low pass filter with a 1:1 RF transformer, allowing the acquisition of sine-wave signals up to 500 MHz in order to increase the input bandwidth and to expose the jitter effect. In this regard, the sampling and hold has a bandwidth of 750 MHz.

IV. RESULTS

All the results presented in common mode are already scaled by −3 dB in order to analyze the noise of one ADC channel.

A. Additive noise input stage

Figure 4 shows the power spectral density of the voltage noise obtained by connecting the two ADC inputs to ground through a 50 Ω resistor, [$v(t) = 0$ V, $f_s = 125$ MHz].

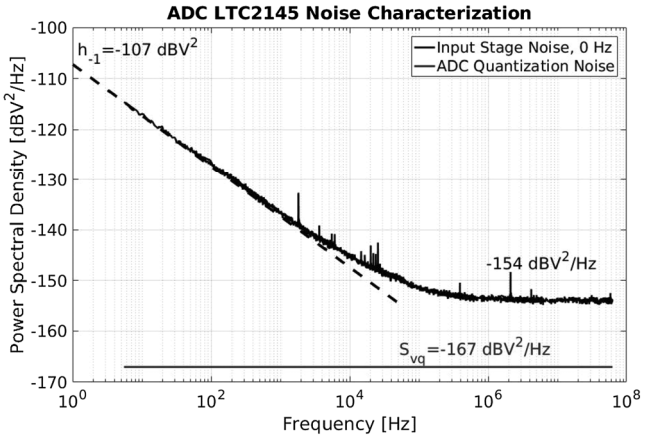

FIG. 4. Power spectral density of ADC LTC2145 input stage noise. The measurement was performed connecting the input to ground through a 50 Ω resistor.

As described in Sec. II, this noise corresponds to the voltage error induced by the input stage. It presents an additive white noise of −154 dBV^2/Hz and an additive flicker of −107 dB V^2/Hz at 1 Hz. The quantization noise floor for the ADC under these conditions (14 bits and 2 V full scale) is −167 dB V^2/Hz.[27] The difference between this value and the estimated white noise floor is 13 dB, in agreement with the effective number of bits (ENOB) stated in the ADC datasheet (11.8).

B. PM measurements

The measurements analyzed in this section were performed acquiring the zero-crossings of the input signal. The voltage noise generated in these samples is induced by the additive noise of the input stage and by the aperture jitter multiplied by the slew rate, as described in (7). These two contributions can be discriminated by varying the amplitude and the frequency (i.e., the slew rate) of the input signal: for low slew rate, the additive noise dominates, while at high slew rate, the measure is representative of the aperture jitter.

Figure 5(a) shows the ADC phase noise ($S_{\tilde{v},\varphi}$) estimated at different input frequencies and 0.9 V of peak amplitude. It can be observed that under these conditions the phase noise is independent of the carrier frequency; the white noise floor differences between each curve are due to aliasing caused by the down sampling performed in order to take only one sample per period. They correspond to aliased φ-type, phase noise caused by random fluctuations in the input stage circuit,[28] where the variations are proportional to the ratio between the analog bandwidth B (for the case of the ADC LTC2145 is 750 MHz) and the phase noise bandwidth (actual Nyquist frequency, $\frac{f_{clk}}{2M}$, according to the input frequency). On the other hand, the flicker phase noise is constant for all the input frequencies being the signature of pure φ-type noise, because it is not affected by aliasing. Figure 5(b) shows the comparison between the additive noise of the input stage (measured with no signal at the input) and the zero-crossings noise induced by acquiring a sine-wave input with a frequency of 125 MHz and an amplitude of 0.9 V. These two noise spectrums are approximately equal. It suggests that the phase noise is dominated by the additive noise of the input stage and that this noise source is independent of the operation point. This is verified later on with the AM measurements. Furthermore, it confirms the assumption that, in this case, the parametric noise of the input stage is negligible with respect to the additive noise.

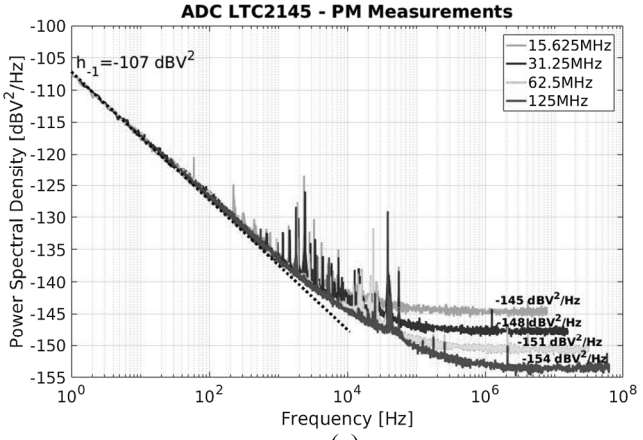

FIG. 5. (a) Power spectral density of ADC phase noise. The contributions of the input stage noise plus aperture jitter are shown. The measurements were taken at different carrier frequencies. The white phase noise level changes due to the aliasing introduced by the down sampling realized in order to take one sample per period at each carrier frequency. (b) Input stage noise and aperture jitter comparison. The phase noise introduced by the ADC is dominated by the additive noise of the input stage which is independent of the carrier frequency.

In order to expose the aperture jitter, the frequency input was increased, augmenting the slew rate. Figure 6 shows the comparison between the PSD of the phase noise estimated at three different carrier frequencies: 125 MHz, 250 MHz, and 500 MHz. The contribution of the aperture jitter can be appreciated from 250 MHz, especially in the flicker region, and it is more evident at 500 MHz. For frequencies higher than the sampling clock, the phase noise bandwidth remains at the maximum value (M equal 1 for these cases); therefore, the white phase noise floor reaches the minimum value. From these results we notice that the voltage noise induced by the aperture jitter starts to emerge at $\nu_0 = 250$ MHz. The contribution of the aperture jitter can be estimated by subtracting the additive noise from the measures done at $\nu_0 = 250$ MHz and at $\nu_0 = 500$ MHz (Fig. 7). The ADC aperture jitter presents a white phase-time noise of −350 dBs^2/Hz for $\nu_0 = 500$ MHz,

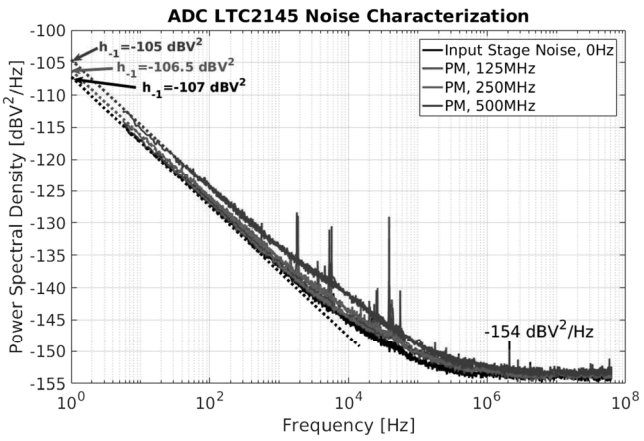

FIG. 6. Power spectral density of voltage noise induced in ADC conversion by phase and time fluctuations. The acquisitions were performed with ν_0 from 125 MHz to 500 MHz. The contribution of aperture jitter emerges at $\nu_0 = 250$ MHz.

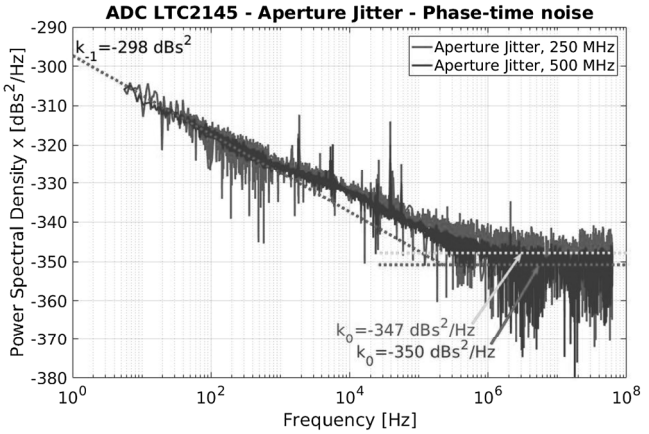

FIG. 7. Power spectral density of ADC aperture jitter. The aperture jitter is revealed from ν_0 = 250 MHz. This result was obtained by subtracting the input stage noise from the ADC phase noise measured at zero-crossings. The obtained aperture jitter is differential and not absolute because of the common noise cancellation. The time jitter rms (J) is around 25 fs_{rms} related to the silicon, consistent with the datasheet information providing the absolute value of 100 fs_{rms}.

decreasing proportionally with the input frequency. According to the datasheet of the ADC LTC2145,[30] the aperture jitter is 100 fs_{rms}, which corresponds to a white noise of −338 dBs^2/Hz. The discrepancy could be due to the common noise rejection, estimating the residual aperture jitter for a single ADC channel. Additionally, the aperture jitter exhibits a flicker phase-time noise of −298 dBs^2/Hz at 1 Hz ($\sqrt{k_{-1}}$ = 1.3 fs), constant with respect to the frequency, signature of pure x-type noise.[28]

The previous results were obtained from the analysis of a series of spectra changing the input frequency, which confirm the presence of the two noise contributions. A similar analysis is performed in Fig. 8, but changing the input amplitude instead of the input frequency. Figure 8 shows the total ADC phase noise ($S_{\varphi,s}$) at ν_0 = 500 MHz when the aperture jitter is starting to emerge. It is seen that the total ADC phase noise is strongly dominated by the additive noise of the input stage, even if the aperture jitter is revealed. Moreover, it increases proportionally to $1/V_0^2$, as expected according to the model (7). From the results, reported in the precedent figures, the ADC LTC2145 has an ultimate phase noise floor of −153 $dBrad^2/Hz$ (white) and −106 $dBrad^2/Hz$ at 1 Hz given by the additive noise of the input stage under maximum sampling frequency and full input voltage range. This noise floor agrees with the results presented in Ref. 21.

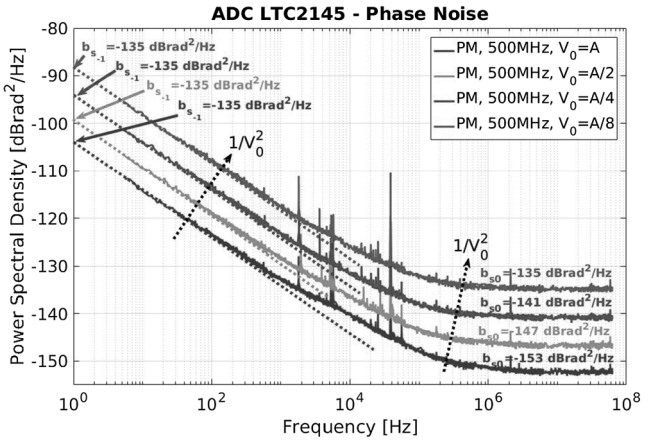

FIG. 8. Sensitivity of ADC phase noise to input amplitude.

C. AM measurements

According to the model, the amplitude noise of the ADC is the superposition of the amplitude noise generated by the input stage and the voltage reference noise. Since the maximum voltage error induced by these noise contributions is generated at the points of maximum amplitude, they can be detected by sampling the peaks of the sine-wave. In order to guarantee the acquisition of these points, an input sine-wave of 31.25 MHz was used, i.e., quarter of the sampling clock (M = 4).

Figure 9 shows the comparison between the PSD of the voltage error estimated under the three measurement conditions: with no signal at the input ($S_{\tilde{v}}$), at zero-crossings ($S_{\tilde{v},\varphi}$), and at peak values ($S_{\tilde{v},\alpha}$). The results in common mode, depicted in Fig. 9(a), suggest that the ADC amplitude noise is also dominated by the additive noise of the input stage.

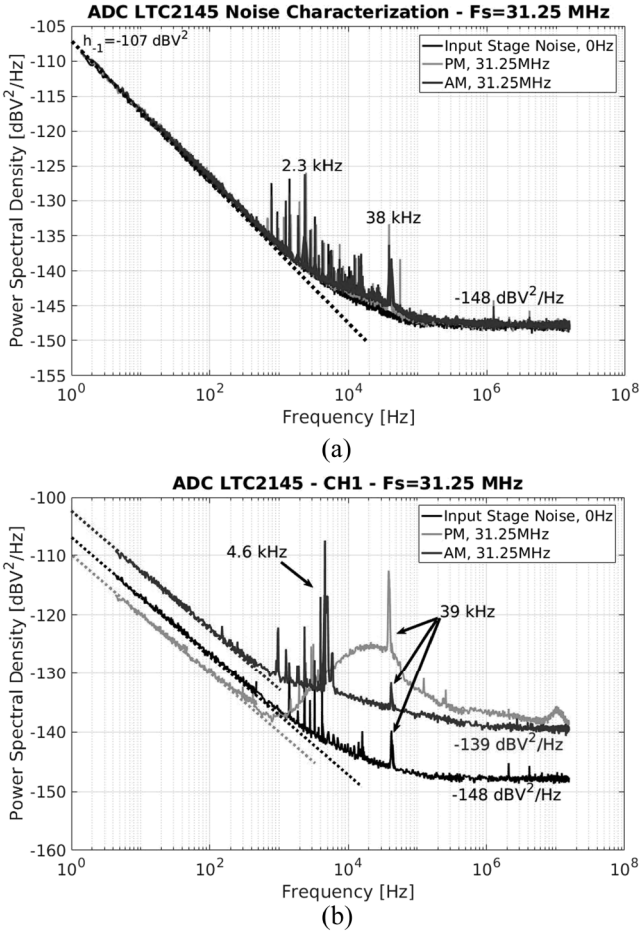

FIG. 9. Comparison of PM and AM measurements. (a) Common mode. The AM and PM noise are similar, suggesting that the input stage noise is equally distributed between the phase and amplitude noise. (b) Differential mode channel 1. The zero-crossings and the maximum amplitude samples were well discriminated. While in zero-crossings is evidenced the feedback loop bandwidth (39 kHz), in maximum amplitude measurements this contribution is not observed.

However, in order to confirm that the AM and PM measurements were done at the proper operation point, Fig. 9(b) shows the PSD of the voltage noise before the common noise rejection, i.e., in single channel. It can be noticed that the contributions of the PI and the feedback loop bandwidth (39 kHz) are evidenced in zero-crossings (PM), while at the peak values (AM) and with no input signal they are negligible. Instead of that, harmonic contributions at 4.6 kHz are observed which might be caused by the signal generator and that are also rejected in common mode. These results confirm the capability of the method for discriminating the operation point (zero-crossings or peak values).

Figure 10 depicts the comparison between the amplitude noise estimated using two different synthesizers for generating the 31.25 MHz input sine-wave, the Agilent E8257D, and the Hewlett Packard 8640B. From the differential mode results [Fig. 10(b)], it is seen that the harmonic contributions around 4.6 kHz were caused by the synthesizer and that although one induced a higher voltage error than the other, the common mode configuration rejected their contributions [Fig. 10(a)] reaching the ADC noise floor.

In order to verify the impact of the voltage reference noise, first it was measured through a fast Fourier transform spectrum analyzer, and afterwards it was compared with the estimated PSD of the amplitude noise. In order to perform properly this comparison, the transfer factor of this noise source on the ADC output was calculated adding an external sine-wave of 1 kHz to the internal voltage reference and measuring the impact on the ADC data for a 31.25 MHz, 0.9 V peak amplitude input signal. This measurement confirmed the equation stated in (7), where the transfer factor is 1. The comparison was done directly and the results are shown in Fig. 11. As can be seen, the voltage reference noise is lower than the voltage error generated by amplitude fluctuations in the input stage. The residual voltage reference noise of each channel after the common noise rejection is expected to be even lower, and it seems not being a limiting factor for the ADC amplitude noise.

Additionally, an analysis for assessing the properties of the ADC amplitude noise ($S_{\alpha,s}$) was performed, similar to the one reported for ADC phase noise. A first series of spectra were obtained by changing the input amplitude, from A (0.9 V) to A/8 (112.5 mV). From Fig. 12(a) it is seen that the amplitude noise is dependent on the input amplitude, as expected from the model (7). A second series of spectra were analyzed, this time changing the input frequency from 15.125 MHz to 31.25 MHz. For the analysis of AM noise, the input frequency cannot be increased beyond quarter the sampling clock in order to guarantee the acquisition of the peak values. Figure 12(b) reports the PSD of the amplitude noise obtained. It exhibits the same behavior of the phase noise generated by the input stage. It confirms that the noise generated by the additive noise of the input stage is independent of the operation point and its effects are similar on amplitude and phase noise.

D. Interpretation of the ADC noise spectra

Table I reports the set of polynomial law coefficients that describes the ADC LTC2145 noise according to the model stated in (7) and based on the characterization results. These features can be compared with the performance of a generic analog mixer which has a flicker phase noise around −140 dB rad^2/Hz at 1 Hz.[31]

However, since this work aims to extract the ADC information which allows predicting ADC noise effects on

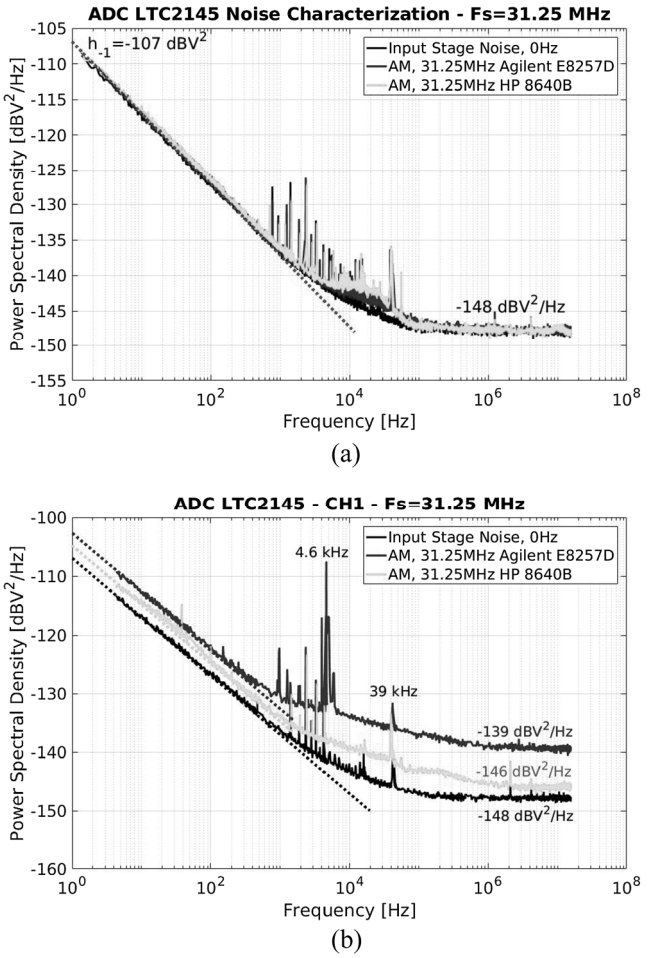

FIG. 10. (a) AM in common mode. ADC AM noise comparison using two signal generators. The amplitude noise generated by the ADC was estimated at the maximum amplitude points of the sine-wave input signal where the effects of this noise are higher. (b) AM in single channel - Channel 1.

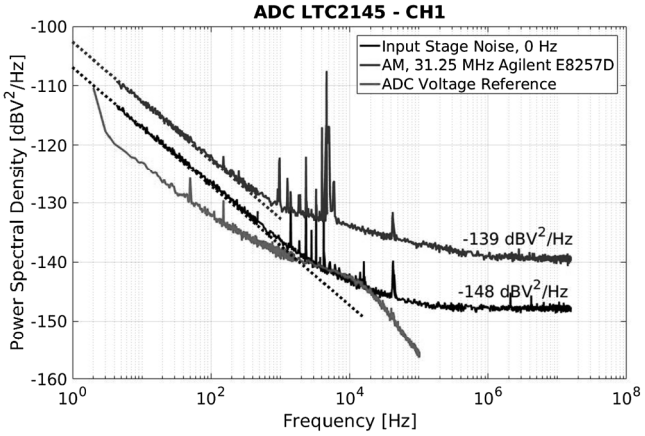

FIG. 11. Voltage reference noise and its effect in single channel. It is seen that the amplitude noise generated by the input stage circuit is higher than this noise contribution, and its effect is rejected in common mode.

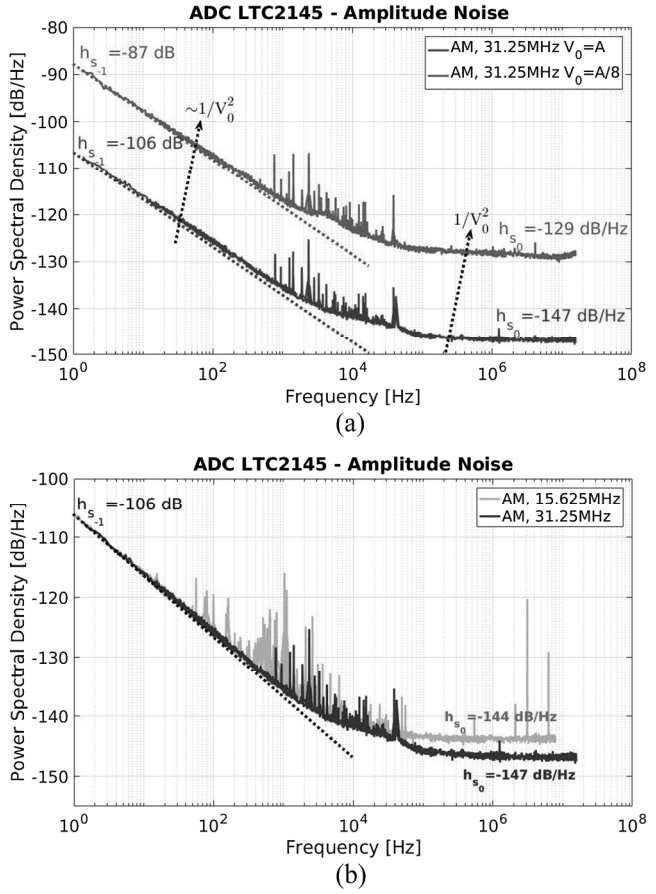

FIG. 12. (a) ADC Amplitude noise dependency with respect to input amplitude. (b) AM noise dependency with respect to input frequency. In agreement with the ADC noise model, the ADC amplitude noise is dependent on the input amplitude and independent of the input frequency. The noise is dominated by the fluctuations generated by the additive noise of the input stage, which causes similar effects on the ADC phase and amplitude noise.

phase/amplitude noise metrology, more general parameters are required. Referring to the study of phase noise and jitter in digital electronics[28] and according to the model proposed here, Table II reports the main general ADC LTC2145 noise parameters obtained from the results shown in Table I. Once

TABLE I. ADC noise model polynomial law coefficients. The boldface values indicate the input conditions at which each noise component was extracted.

Noise source	White noise	Flicker noise at 1 Hz
Phase noise		
$S_{\varphi,s}(f) \approx \frac{1}{V_0^2} S_{n_\varphi,s}(f)$	$b_{s_0} = -153$ dBrad^2/Hz **ν_0 = 125 MHz, V_0 = 0.9 V**	$b_{s_{-1}} = -106$ dBrad^2 **ν_0 = 125 MHz, V_0 = 0.9 V**
$S_{x,s}(f)$	$k_0 = -350$ dBs^2/Hz **ν_0 = 500 MHz**	$k_{-1} = -298$ dBs^2 **ν_0 = 500 MHz**
Amplitude noise		
$S_{\alpha,s}(f) \approx \frac{1}{V_0^2} S_{n_\alpha,s}(f)$	$h_{s_0} = -148$ dB/Hz **ν_0 = 31.25 MHz, V_0 = 0.9 V**	$h_{s_{-1}} = -107$ dB **ν_0 = 31.25 MHz, V_0 = 0.9 V**
$S_r(f)$	$h_{r_0} = -156$ dB/Hz **ν_0 = 31.25 MHz**	$h_{r_{-1}} = -116$ dB **ν_0 = 31.25 MHz**

TABLE II. ADC noise parameters.

Parameter	Square root value ADC LTC2145 common mode
$h_0 B = \frac{b_{s_0} f_s V_0^2}{2}$	$\sqrt{h_0}\,B = 159\,\mu V_{rms}$
$h_{-1} = b_{s_{-1}} V_0^2$	$\sqrt{h_{-1}} = 4.5\,\mu$V
$J^2 = k_0$ [a] $\frac{f_s}{2}$	$J = 25$ fs$_{rms}$
k_{-1} [b]	$\sqrt{k_{-1}} = 1.3$ fs

[a] $b_{x_0} = \frac{8\pi^2 \nu_0^2 J^2}{f_s}$.
[b] $b_{x_{-1}} = 4\pi^2 \nu_0^2 k_{-1}$.

these parameters are obtained ($h_0 B, h_{-1}, J, k_{-1}$), since they are generic values for this particular ADC, they can be used for re-estimating the ADC phase noise spectra and calculating the corresponding power law coefficients ($b_{s_0}, b_{s_{-1}}$) for an input signal of interest (ν_0, V_0, f_s). For instance if the noise of an oscillator of 10 MHz is intended to be measured, the ADC will have a phase noise floor given by $b_{s_0} = -153$ dB rad^2/Hz and $b_{s_{-1}} = -106$ dBrad^2. The aperture jitter will not limit the measurement having a phase noise given by $b_{x_0} = -194$ dBrad^2/Hz and $b_{x_{-1}} = -142$ dBrad^2. In general, 10 MHz commercial low noise crystal oscillators exhibit phase noise floors below −110 dBc/Hz at 1 Hz and −158 dBc/Hz white noise far from the carrier;[32] therefore, techniques for ADC noise rejection should be applied in order for the instrument not to limit the oscillator phase noise measurement. Based on the ADC characterization, the rejection level can be determined.

V. CONCLUSIONS

The main noise sources of a high resolution, two-channel ADC are exposed through a low computational cost method by acquiring synchronously two operation points of a sine-wave input signal: zero-crossings and peak values. From the measurements in single channel and in common mode, we have verified the proper discrimination of each operation point and the lack of correlation of the two ADC channels. According to their analysis, we conclude that the phase and the amplitude noise are limited by the additive noise generated in the input stage, which impacts similarly in these two ADC noise components (phase and amplitude). The voltage reference does not degrade the ADC acquisition even at the maximum input voltage range. Albeit the aperture jitter does not have a high impact on the ADC phase noise in common mode, we could verify its properties and behavior. From these results we can claim that the ADC phase noise effects are lower at high sampling frequency and high input amplitude.

The technique for ADC noise characterization proposed here provides estimated amplitude and phase noise floors at frequency offsets close (down to 10 Hz) and far to the carrier (up to Nyquist frequency) which allows direct analysis for phase and amplitude noise metrology. It can be replicated for characterizing any high resolution ADC. The requirements are two-channel ADC, one DAC, and a digital PI. For the nature of the digital processing, the computational resources needed are not high: RAM blocks of 16 kB per channel and digital clock

system at the maximum of the ADC sampling clock were used in the setup presented.

This work presents a differential ADC noise model, rejecting the common noise contributions. Alternatively, Non-Linear Transmission Lines (NLTL) could be used[33] for changing the slew rate and for obtaining an absolute or complete ADC noise model.

The proposed ADC characterization allows having access to the main ADC noise sources in order to predict the effects on phase noise measurements, useful information for the phase noise metrology instrumentation design. Based on that, we can claim that high resolution ADCs are suitable for implementations at high frequency and high input amplitude. Albeit their phase noise could limit phase noise measurements of low noise oscillators, knowing the ADC noise properties could open the door to new techniques for ADC noise rejection on amplitude and phase noise metrology.

Extensions of this work could include noise characterization of high resolution ADCs of different architectures and technologies, and the assessment of two-channel ADCs not embedded in the same chip where common noise rejection is expected to be lower.

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