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Accessing ratios of quantized resistances in graphene p-n junction devices using multiple terminals / Patel, Dinesh; Marzano, Martina; Liu, Chieh-I; Hill, Heather M.; Kruskopf, Mattias; Jin, Hanbyul; Hu, Jiuning; Newell, David B.; Liang, Chi-Te; Elmquist, Randolph; Rigosi, Albert F.. - In: AIP ADVANCES. - ISSN 2158-3226. - 10:2(2020), p. 025112. [10.1063/1.5138901]

Availability:

This version is available at: 11696/64709 since: 2020-12-23T10:56:17Z

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DOI:10.1063/1.5138901

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Cite as: AIP Advances **10**, 025112 (2020); <https://doi.org/10.1063/1.5138901>

Submitted: 15 November 2019 . Accepted: 19 January 2020 . Published Online: 07 February 2020

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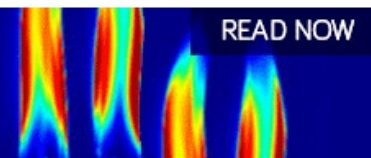
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Submitted: 15 November 2019 • Accepted: 19 January 2020 •

Published Online: 7 February 2020



Dinesh Patel,^{1,2} Martina Marzano,^{1,3,4} Chieh-I Liu,¹ Heather M. Hill,¹ Mattias Kruskopf,^{1,5} Hanbyul Jin,^{1,5} Jiuning Hu,^{1,5} David B. Newell,¹ Chi-Te Liang,² Randolph Elmquist,¹ and Albert F. Rigosi^{1,a)}

AFFILIATIONS

¹Physical Measurement Laboratory, National Institute of Standards and Technology (NIST), Gaithersburg, Maryland 20899-8171, USA

²Department of Physics, National Taiwan University, Taipei 10617, Taiwan

³Department of Electronics and Telecommunications, Politecnico di Torino, Torino 10129, Italy

⁴Istituto Nazionale di Ricerca Metrologica, Torino 10135, Italy

⁵Joint Quantum Institute, University of Maryland, College Park, Maryland 20742, USA

^{a)}Author to whom correspondence should be addressed: albert.rigosi@nist.gov

ABSTRACT

The utilization of multiple current terminals on millimeter-scale graphene p - n junction devices has enabled the measurement of many atypical, fractional multiples of the quantized Hall resistance at the $\nu = 2$ plateau ($R_H \approx 12\,906\,\Omega$). These fractions take the form $\frac{a}{b}R_H$ and can be determined both analytically and by simulations. These experiments validate the use of either the LTspice circuit simulator or the analytical framework recently presented in similar work. Furthermore, the production of several devices with large-scale junctions substantiates the approach of using simple ultraviolet lithography to obtain junctions of sufficient sharpness.

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Graphene, composed of carbon atoms arranged in a two-dimensional honeycomb lattice, has been extensively studied for more than a decade, in part because of its excellent optical, mechanical, and electrical transport properties.^{1–4} The quantum Hall effect (QHE) in graphene gives resistance values at $\frac{1}{(4n+2)}\frac{h}{e^2}$, where n is an integer, h is the Planck constant, and e is the elementary charge. Graphene p - n junctions (pn Js), which are suitable for one to explore transport in the QHE,^{5–18} enable one to access various multiples and fractions of the von Klitzing constant. These types of graphene devices also have additional applications in electron optics,^{19–22} photodetection,^{23–27} and quantum Hall resistance standards.^{28–38}

For clarity, a pn J device contains some form of interface at which a positively doped and a negatively doped region meet. For graphene, whose Fermi level can be electrically or chemically

modulated, such an interface can be effectively one-dimensional, allowing edge state electrons to tunnel from one region to the other. This behavior results in the observation of quantized longitudinal resistances due to the presence of the junction. Typically, these devices are of sub-millimeter sizes due to constraints on top-gating. One motivation for pursuing large-scale pn J devices is to determine the feasibility of using quantum transport across the junctions to access different quantized values of resistance, as shown in previous studies.^{39–41} One first major hurdle is to fabricate large-scale devices without the need for top-gating, since such techniques become more complicated as the device incorporates more elements. Although extensive analyses exist on Landauer–Büttiker edge state equilibration,^{5–8,42–46} creating a pn J device capable of accessing different plateaus with top gates is a difficult task. Instead, one approach to accessing different quantized values is to incorporate multiple

current terminals, which opens the parameter space within which pnj devices are able to be operated.

For millimeter-scale device fabrication, epitaxial graphene (EG) is grown to accommodate device size, but the issue of processing the correspondingly large pnj s was not trivial, as shown in previous work.⁴⁷ This work elaborates on further efforts involving the use of standard ultraviolet photolithography (UVP) and ZEP520A to build pnj s having widths smaller than 200 nm. Devices were verified via quantum Hall transport measurements and LTspice current simulations,⁴⁸ and multiple current terminals and configurations were used to test the viability of the simulations as well as the quality of the devices. Furthermore, recently reported analytical methods were also used to predict atypical fractions of the quantized Hall resistance, R_H , that would become experimentally accessible depending on the configuration of the current terminals.⁴⁹ These experiments also serve as supporting evidence on the validity of those analytical methods, which provide easily implementable algorithms for determining effective quantized resistances in complicated pnj circuits.

Simulations for the pnj devices were performed with the analog electronic circuit simulator LTspice in an identical manner as demonstrated for similar devices in other works.^{47,49–51} The circuit

uses both p -type and n -type k -terminal quantum Hall elements, designated as either having ideal counterclockwise (CCW) or clockwise (CW) edge state current flow. EG on SiC was fabricated into pnj devices after the growth at a temperature of 1900 °C. First, chips were diced from 4H-SiC(0001) wafers (CREE)⁴⁸ and chemically cleaned with a 5:1 diluted solution of hydrofluoric acid and deionized water. Just prior to growth, chips were processed with AZ5214E to utilize polymer-assisted sublimation.⁵² Finally, after placing the chips on a polished graphite substrate (SPI Glas 22)⁵⁰ silicon-face down, the growth occurred under an ambient argon environment at 1900 °C with a graphite-lined resistive-element furnace (Materials Research Furnaces, Inc.).⁴⁸ The corresponding heating and cooling rates of the furnace were about 1.5 °C/s.

Once grown, EG was assessed with confocal laser scanning, optical, and atomic force microscopy (AFM).⁵³ Images acquired from these techniques are provided in Fig. 1, which confirmed that homogeneous monolayer EG had successfully covered millimeter-scale areas (see the [supplementary material](#) for additional AFM images). Next, using Pd and Au as protective layers against organic contamination, photolithographic processes were performed, details of which may be found in other works.^{31,47} Once each Hall bar device was completed, it underwent $\text{Cr}(\text{CO})_3$ functionalization to reduce

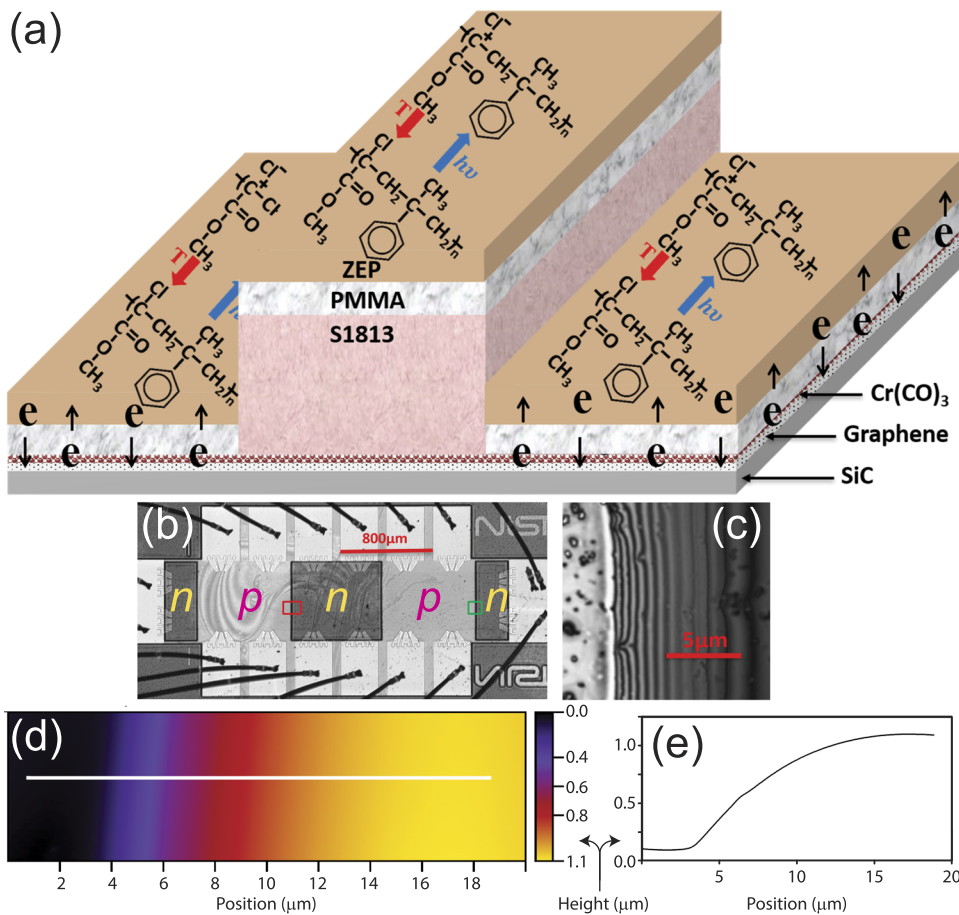


FIG. 1. (a) An illustration of the surface of an EG pnj device. The photoresist S1813 was deposited and lithographically processed on specific regions where n -type doping was preferred. The molecule in ZEP520A is shown to clarify the electron acceptor as the photoresist is exposed to ultraviolet light. $\text{Cr}(\text{CO})_3$ was used to stabilize the electron density. (b) A confocal microscope image acquired for the full device after wire bonding, with the darker region indicating the desired n -type regions. (c) A magnification of the small green box in (b) for a scale of the order of 5 μm. Oxidized residue from the $\text{Cr}(\text{CO})_3$ deposition takes the form of visible black specs. (d) and (e) show both the two-dimensional and one-dimensional height profiles, respectively, with the one-dimensional profile represented as a white line in (d) and the two-dimensional profile acquired within the red box in (b).

the electron density to approximately 10^{10} cm^{-2} .^{54–58} The major final steps included the deposition of S1813 photoresist as a spacer layer for intended *n*-type regions, PMMA/MMA photoresist as an additional spacer, and ZEP520A as a photoactive layer, as described in the literature.^{47,59} Uniformity is also verified with Raman spectra (see the [supplementary material](#)).

Although AFM images suggest a sloped S1813 spacer layer, preservation of the *n*-type regions can still be accomplished with thicknesses of the order of 100 nm.⁴⁹ Furthermore, the upper bound of the junction width resulting from these photolithographic processes was measured to be approximately 200 nm in another work, rendering them of sufficient sharpness to accommodate edge-state propagation.⁴⁹ Ultraviolet (UV) light, with a wavelength of 254 nm, was used to realize *p*-type doping in regions without S1813. The longitudinal resistivity was monitored during periods of UV exposure, and additional information and data on this process are found in the [supplementary material](#).

Completed four-junction devices, like the one shown in [Fig. 1\(c\)](#), were measured with the traditional methods to verify that regions exhibited resistance quantization. This type of device is shown in [Fig. 2\(a\)](#). Electrical contact pads are numbered based on the measurement system used to provide the corresponding measurements in (b) and (c). Traditional longitudinal and Hall measurements were acquired at 1.6 K and ± 9 T, with the results shown in [Fig. 2\(b\)](#) as black and red curves, respectively. With proper UV

exposure, regions without the S1813 spacer layer are subject to *p* doping, and after sufficient exposure time, they become set as *p*-type regions.

The resulting *pn*Js were found to be of sufficient narrowness to accommodate dissipationless edge-state propagation.⁴⁷ However, to further verify that the entire device was functional, voltage measurements were performed along the length of the device, bearing in mind the formation of the device's so-called hot spots, as shown pictorially in [Ref. 40](#). In [Fig. 2\(c\)](#), the plotted resistances further support the idea that millimeter-scale *pn*Js can be successfully fabricated with standard UV lithography.

A recent formulation for using multiple terminals on a *pn*J device as the only resistive elements of a circuit has established a mathematical way of predicting the effective quantized resistance of that circuit.⁴⁹ Essentially, a single current source can inject current into an arbitrary number of terminals—likewise for the drain port of the current source. The voltage difference of the whole circuit, and by extension the effective quantized resistance $R_{\text{eff}} = q_{N-1}R_H$, can then be measured between just after the current source starts and just before the drain of the current source terminates. The coefficient of effective resistance (CER) is labeled q and represents a device configuration containing N total terminals that are used (either as a source or as a drain).

Eight different configurations were measured, and their effective circuit resistances are plotted in [Fig. 3](#). Furthermore, two meth-

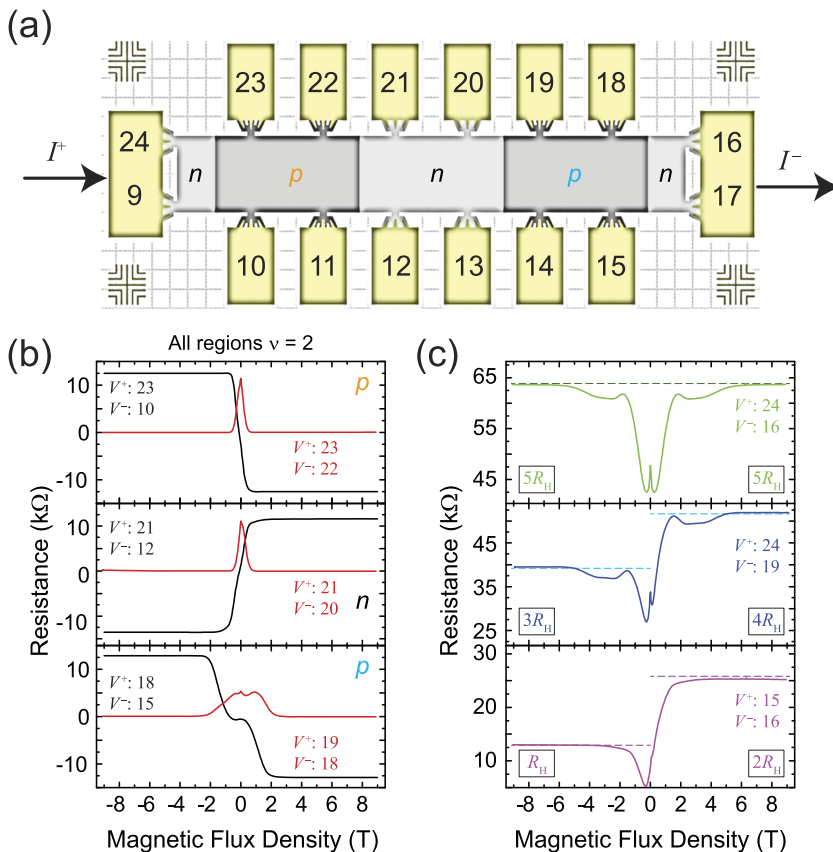


FIG. 2. (a) A four-junction device illustration with numbers corresponding to wired connections on a 32-pin leadless chip carrier, with the electron flow entering from the right-side contact (drain) and with the source on the left side. A current of $1 \mu\text{A}$ was applied for all measurements. Darker and lighter gray colors indicate *p*-type and *n*-type regions, respectively. The three middle regions are tested to check traditional Hall resistance curves, with orange and cyan *p* labels matching those seen in (b). (b) The longitudinal and Hall resistances were measured from 9 T to -9 T at 1.6 K and are represented by red and black curves, respectively. Pin labels are also provided. (c) Integer multiples of R_H (from 1 to 5) were measured across varying lengths of the device to ensure device functionality. Dotted lines are provided as a visual guide to compare exact quantized values. All regions were on the $\nu = 2$ plateau.

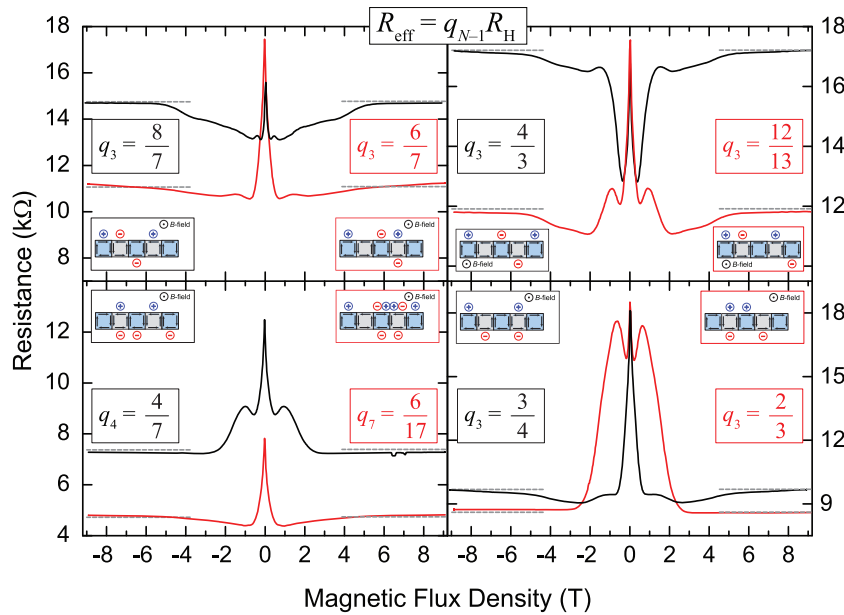


FIG. 3. Multiple-terminal configurations have been measured and their effective circuit resistances are plotted in the four panels. Three of the four panels contain four-terminal configurations (two sources and two drains), whereas the panel on the lower left corner uses a five-terminal and an eight-terminal configuration. The latter panel, when compared with the calculated and simulated value in dotted gray lines, provides some evidence that the CER formulation is valid for larger numbers of used terminals. All panels contain the calculated and simulated value in dotted gray lines (valid for sufficiently high magnetic flux density), and for all cases, the calculated and simulated results agree with each other. The insets of each panel have colored perimeters corresponding to the curve of the same color and illustrate the four-junction device and its edge-state current flow abstractly. The blue plus and red minus signs indicate source and drain terminals, respectively.

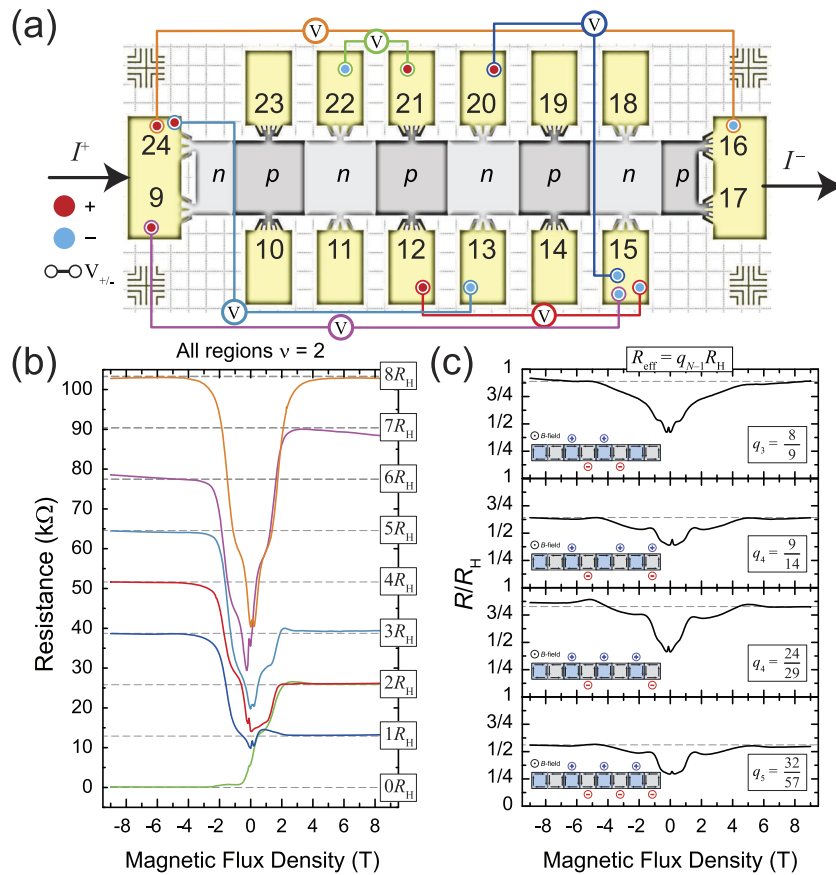


FIG. 4. (a) A seven-junction device illustration with numbers corresponding to the same measurement system is shown using a measurement current of $1 \mu\text{A}$. Darker and lighter gray colors indicate p -type and n -type regions, respectively. Each measurement pair is color-coded for easy comparison to its corresponding data. (b) The resistance is plotted for each of the voltage measurement pairs in (a) with the same color-coding used to match the illustration. The dotted gray lines represent the exact values of the multiples of R_H . All regions were on the $\nu = 2$ plateau. (c) Several new configurations were measured and compared with both simulations and the CER formulation, with the latter two in exact agreement. Thus, both theoretical values are represented by the same gray dotted line in each of the four panels. On the bottom left of each graph panel, the illustrated device is shown with the corresponding locations of sources (blue plus symbol) and drains (red minus symbol) along the device. Voltages were measured from the point before the sources split to the point after the drains rejoin, yielding the CERs of each configuration.

ods were used to predict the expected CERs of the circuit—the LTspice simulator and the CER formulation. Both methods agreed exactly and are plotted as gray dotted lines for each of the eight configurations. The crucial formula used to mathematically predict the expected CERs⁴⁹ is as follows:

$$q_{N-1}(n_{N-1}) = \frac{q_{N-2}(n_{N-1} + 1)}{n_{N-1} + \frac{q_{N-2}}{q_{N-1}}}. \quad (1)$$

The CERs calculated in Fig. 3 include the following: $\{\frac{6}{7}, \frac{8}{7}, \frac{12}{13}, \frac{4}{3}, \frac{6}{17}, \frac{4}{7}, \frac{3}{4}, \frac{2}{3}\}$. Details on how to proceed with the calculation are well-documented in Ref. 49, and additional examples for some of the configurations in this manuscript are found in the [supplementary material](#).

To demonstrate how increasingly complex calculations can yield atypical CERs, devices containing seven pn s were fabricated as shown in Fig. 4(a). Although even more pn s can be placed along the 2 mm length of the device, their number was limited by the preference of accessing each region with an electrical contact for proof of concept. Figure 4(a) shows voltage leads of varying color that were used for determining the resistance curves and by extension the CERs [Fig. 4(b)].

Sufficient quantization was seen for the more traditional cases of measuring the resistance across parts of the device while the source and drain are at the farthest terminals. All integer multiples of R_H between 1 and 8 were accessible in this characterization, warranting further measurements with multiple terminals. In Fig. 4(c), four configurations were measured using different numbers of total terminals. The top panel, using four terminals as illustrated in the inset, yielded data that were then compared to the predicted CER of $q_3 = \frac{8}{9}$. The two middle panels used five terminals and were compared with their corresponding predicted values of $q_4 = \frac{9}{14}$ and $q_4 = \frac{24}{29}$. In the bottom panel, the six-terminal configuration was measured and compared with its corresponding prediction of $q_5 = \frac{32}{57}$. For the sake of clarity and as an additional tutorial, this fourth case is calculated in more detail in the [supplementary material](#). Overall, such devices and their CERs can be measured for many configurations of similar or greater complexity. Moreover, desired, user-specific CERs can be reversed engineered into a corresponding configuration.

In conclusion, this work pursued further efforts involving pn devices fabricated from EG on SiC with junction widths sufficiently narrow to observe usual edge-state propagation. By configuring an experimental setup to include multiple sources and drains, various atypical quantized resistances became accessible and matched predicted values based on LTspice simulations. Additionally, recently reported analytical methods were also used to support the predicted values of the same atypical fractions of R_H . The results demonstrate that pn s have the potential to bring scalable resistance values as well as reinforce the validity of the aforementioned CER formulation, which provides a simple algorithm for determining the effective quantized resistances in pn circuits.

See the [supplementary material](#) for the details on UV exposure and for additional calculations.

The work of D.K.P. at NIST was made possible by C.-T. Liang of National Taiwan University. The work of M.M. at NIST was made possible by M. Ortolano of Politecnico di Torino and

L. Callegaro of Istituto Nazionale di Ricerca Metrologica, and the authors thank them for this endeavor. The authors would like to thank T. Oe and X. Wang for their assistance in the NIST internal review process.

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