Measurement of the Absolute Phase Error of Digitizers

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Abstract—This paper proposes a method for the measurement of digitizer absolute phase errors, defined as the phase displacement between the digitized output and the input analog waveform. The measurement procedure is based on the use of a phase reference signal (PRS), which is theoretically synchronous with the input analog waveform and that triggers the digitizer sampling clock. From the characterization of the waveform generator phase response and the measurement of the time delay of the digitizer sampling clock with respect to the PRS, an accurate evaluation of the digitizer absolute phase error is obtained. The method has been applied to a high-performance digitizer, measuring the absolute phase errors of two different channels. The expanded uncertainty of the method has been quantified as a few microradians at 50 Hz and 150 μrad at 20 kHz.

Index Terms—Calibration, Digital Low-Power Instrument Transformer (DLPT), digitizer, Discrete Fourier Transform (DFT), phase measurement, Phasor Measurement Unit (PMU), power system measurements.

I. INTRODUCTION

The knowledge of phase angles of signals is at the base of many engineering applications, from telecommunications to power systems [1], [2]. In particular, in most measurement applications, electronic instrumentation is based on digitizers to convert analog signals to digital samples that are handled by digital signal processors to get the desired measurement value. However, every digitizer has its own phase frequency response which introduces a phase deviation, between the analog input and its corresponding digital output samples, that is here defined as the absolute phase error of the digitizer. This deviation depends on the characteristics of the digitizer input circuitry and the digitalization architecture. For very low-frequency signals, this phase deviation can be negligible, if the phase displacement reflects into a time delay much lower than the time period of the considered waveform. For many applications, two channels of the same digitizer are involved in the measurement at the same time (i.e., power, energy, or impedance measurement) so that only the relative phase delay between channels is important. Measuring the relative phase delay between the two channels of the same digitizer, or two channels of two different digitizers with synchronized sampling clocks, is an issue faced in a number of scientific papers [3]–[5]. However, there are special applications, such as high-accuracy calibration of Phasor Measurement Units (PMU) for medium voltage grid application [6]–[10] or calibration of low-power instrument transformers [11]–[14] with digital output (DLPT), carried out by comparison with a standard analog transformer, where high phase accuracies, of the order of the microradian, are required. In these situations, the absolute phase deviation of the single channel of the used digitizer may be comparable or higher than the required accuracy, introducing an unacceptable systematic error that highly influences the measurement result.

An interesting technique for the measurement of digitizer absolute phase error was proposed in [15], which involves the generation of a reference signal with known phase with respect to a time reference, but it is not thoroughly discussed and only first results are shown.

In this paper, a different technique for measuring the absolute phase errors of digitizer is presented. The technique has been introduced in [16], but here a thorough theoretical explanation is given, together with an exhaustive uncertainty analysis and an experimental validation. It is based on the preliminary characterization of the phase error of the used analog waveform generator with respect to a phase reference signal (PRS), through the use of a phase comparator [4], [5]. By means of a frequency counter, which measures the time delay between the sampling clock of the digitizer under test (DUT) and the PRS, and applying the discrete Fourier transform (DFT) to the DUT samples, the absolute phase error of the DUT is measured.

This paper is organized as follows. Section II describes the measurement procedure, whereas Section III focuses on the adopted measurement setup. Section IV analyzes systematic errors and uncertainty contributions. Section V discusses the experimental characterization of a digitizing module, and
Section VI, in order to validate the proposed technique, presents a comparison with results obtained through a phase comparator [3]–[5].

II. MEASUREMENT METHOD

The measurement of the absolute phase error of a digitizer involves the evaluation of a phase delay between a digitized quantity, that is the output samples of the digitizer, and an analog quantity (typically a voltage), that is the digitizer input signal. To the best of the authors’ knowledge, direct measurement methods able to quantify this phase error are not available. Therefore, an indirect measurement method, based on the introduction of a reference phase signal (a square wave), having the same frequency of the input signal, has been adopted.

At first, let consider an arbitrary waveform generator (AWG) that also provides a signal that acts as the PRS. This is a square signal with the same periodicity $T_0$ of the generated sinusoidal signal. When a sinusoidal signal $s_g$ is generated, ideally, the zero crossing of the sine wave and square wave should be at the same time instant. Actually, due to the frequency response of the AWG and to its internal time delay, there is a time delay $T_g$ between the zero crossing of sine wave and the rising edge of square wave. Assuming the rising edge of the PRS as the time reference ($t = 0$), the time delay, which corresponds to an initial phase angle of the sine wave equal to $\phi_g$, is

$$\phi_g(f_0) = \frac{2\pi}{f_0} T_g = 2\pi f_0 \cdot T_g = \omega_0 T_g$$

where $f_0$ is the signal frequency. Thus, the generated sine wave can be written as

$$s_g(t) = \sin(2\pi f_0 t - \phi_g)$$

where for the sake of simplicity, a unitary amplitude is considered. This effect is illustrated in Fig. 1.

Now, let suppose that PRS is used to trigger the starting of the sampling performed by the digitizer (DUT) to be characterized. Ideally, the first command of the sampling should be aligned with the rising edge of PRS, but, due to the delay of the clock paths, it is actually delayed of a time interval $T_c$ (see Fig. 2).

After that, sampling commands are generated equally spaced of the chosen sampling period $T_s$ with the accuracy of the adopted sampling clock (Fig. 2).

In a digitizer, the sampling command should ideally produce an instantaneous acquisition of a sample but, actually, there is always a delay $T_{DUT}^d$ between the sampling command and the acquisition of the sampled value. This delay impacts on the acquired waveform as a phase shift. This, summed to the phase shift $\phi_{DUT}^a$ introduced by the transfer function of the analog input circuitry of the digitizer, determines a phase error, i.e., the absolute phase error of the digitizer ($\phi_{DUT}^a$). Therefore, the absolute phase error of the DUT can be expressed as

$$\phi_{DUT} = 2\pi f_0 T_{DUT}^d + \phi_{DUT}^a.$$ (3)

As a consequence, the time delay between the sampling command and the acquisition of the sampled value is

$$T_{DUT} = \frac{\phi_{DUT}}{2\pi f_0}.$$ (4)

This situation is depicted in Fig. 3.

In order to evaluate the absolute phase error, let suppose that the DUT is supplied with a signal $s_g$ and the PRS triggers...
the sampling performed by the DUT. All the phenomena previously shown occur together, as shown in Fig. 4.

The sinusoidal waveform acquired by the DUT can be expressed as

\[ s_{\text{DUT}}(kT_s) = \sin(2\pi f_0(kT_s + T_c + T_{\text{DUT}} - T_g)) \]

\[ = \sin(2\pi f_0kT_s + \varphi_c + \varphi_{\text{DUT}} - \varphi_g) \]

\[ = \sin(2\pi f_0kT_s + \varphi_f) \]  \hspace{1cm} \text{(5)}

where time delays are given in terms of phase displacements (1). The term \( \varphi_f \) represents the comprehensive effect of all the time delays on the phase displacement of the acquired sinusoid. The phase angle \( \varphi_f \) can be evaluated by performing the DFT on the acquired samples and evaluating the phase angle at frequency \( f_0 \) with a synchronized acquisition or different signal processing techniques. The phase deviation \( \varphi_{\text{DUT}} \), introduced by the DUT at frequency \( f_0 \), can be then obtained by

\[ \varphi_{\text{DUT}} = \varphi_f - \varphi_c + \varphi_g \]  \hspace{1cm} \text{(6)}

where the phase delays \( \varphi_c \) and \( \varphi_g \) are measured as detailed in the following.

III. MEASUREMENT SETUP

To validate the proposed method, a proper automated test bench has been realized. Its block scheme is shown in Fig. 5.

The system is based on a PXI (PCI eXtension for Instrumentation) chassis: a GPS-disciplined Rubidium atomic clock (Fluke 910R) and an external universal frequency counter (Agilent 53230A). The multifunction I/O module National Instruments (NI) PXIe-6124 (±10 V, 16 bit, maximum sampling rate 4 MHz) is the DUT. The module NI PXI-5422 (±12 V, programmable gain, 16 bit, maximum sampling rate 200 MHz) has been used for AWG. The NI PXI 4462 (±10 V, 24 bit, maximum sampling rate of 204.8 kHz) module is used as a phase comparator.

All the instruments of the test bench operate synchronously since the clock source from the Fluke 910R is provided to the whole PXI backplane and to the frequency counter as external time base. Clock signals (with frequency different from 10 MHz) and trigger signals are generated by the NI PXI-6683H synchronization board. In particular, the sampling clock of DUT (C_{\text{DUT}} in Fig. 5), the PRS and the AWG generation clock (C_{\text{AWG}} in Fig. 5, set to 5 MHz) are generated by the NI PXI-6683H. A digital storage oscilloscope (Lecroy MDA810, not shown in Fig. 5) is used to control the right operation of the setup and measure the rise time of the PRS. It is worth to underline that C_{\text{DUT}} is externally provided to the DUT, through the terminal PF10 (Programmable Function Input 0); moreover, the DUT starts to sample when it recognizes the first pulse of the sample clock, which is delayed from PRS of a time \( T_c \) (see Fig. 2).

The AWG, generating the sine wave \( s_g \), is connected to both the DUT and phase comparator (COMP), which measures the phase difference \( \varphi_g \) between \( s_g \) and PRS. The frequency counter gives the time delay \( T_c \) between PRS and DUT sampling clock. All the clock and signal paths are symmetrically managed (as better explained in the following) in order to avoid different propagation delays.

Measurement software is developed in LabVIEW, using the event-based state-machine approach.

For each test point, amplitude and frequency of the test signal of the DUT can be chosen and 30 repeated measurements of \( \varphi_f, T_c \), and \( \varphi_g \) are performed. In order to evaluate \( \varphi_f \), for each test frequency, a time window equal to a fixed number of signal periods is used to perform the DFT.

For the sake of simplicity, in the realized setup, a DUT which accepts external sampling clock is used. However, the proposed method does not lose generality even in the presence of a DUT which accepts the sampling clock through the communication bus (whatever it is), since it is sufficient to access to the pin receiving the sampling clock.

IV. SYSTEMATIC ERRORS AND SOURCES OF UNCERTAINTY

A. Counter and Comparator Interchannel Delay

Both the measurement values given by the phase comparator, \( \varphi_g \), and the frequency counter, \( T_c \), are affected by systematic errors due to differential time delay between the two paths to the channel inputs of the instruments. These systematic effects can be estimated and corrected as briefly described in the following.

Let consider the two input paths of a frequency counter, as depicted in Fig. 6(c): \( t_{\text{a}} \) and \( t_{\text{b}} \) indicate the time delays in propagation due to the cables that connect the signals...
The differential delay of a frequency counter including cables.

![Diagram of a frequency counter with cables](image)

\[ \tau_{ab} = \tau'_a + \tau''_b - (\tau'_b + \tau''_a) \]  

(7)

Fig. 7. Differential delay of a frequency counter including cables.

Similar considerations can be done for the phase comparator, considering now that the signals at its inputs have relative phase delay of \( \Delta \phi_d \). The introduced uncertainty contribution depends on the repeatability and stability of the generated signals. In this case, the systematic effect introduced by the comparator can be modeled with a differential phase displacement \( \Delta \phi_{ab} \).

Performing two measurements, inverting the inputs, (10) is obtained. It results

\[
\begin{align*}
\Delta \phi_1 &= \Delta \phi_{ab} + \Delta \phi_d \\
\Delta \phi_2 &= \Delta \phi_{ab} - \Delta \phi_d
\end{align*}
\]  

(10)

B. Time Delay Between DUT Sampling Clock and PRS

As it is explained in Section II, the rising edge of the PRS is considered as the time reference \( t = 0 \), and, thus, all the measured time or phase delays are referred to it. However, an uncertainty source has to be considered as associated with this assumption that is the fact that the PRS is not an ideal square wave; this aspect particularly affects the measurement of the time delay between the DUT sampling clock and the PRS. In fact, the intrinsic low-pass behavior of the PRS generation affects amplitudes and phases of all harmonic components of the generated square wave, possibly introducing phase delays. Nevertheless, if the analog bandwidth of the PRS generator is sufficiently greater than the fundamental frequency of the generated square wave, the contribution to the total uncertainty, due to this assumption, can be considered small. For the case at hand, the square waves (PRS and DUT sampling clock) are generated by the synchronization board, which is optimized to deal with square waves and has an analog bandwidth of about 50 MHz, whereas the maximum analyzed frequency is 20 kHz, that is more three orders of magnitude lowers. However, measuring the rise time of the PRS, the estimated uncertainty contribution is lower than 0.2 \( \mu \)rad at 50 Hz and 68 \( \mu \)rad at 20 kHz.

C. Phase Delay Between Sine Wave and PRS

From a mathematical point of view, the phase is defined for a sine wave with respect to a time reference. Therefore, the problem of measuring the phase delay between the sine wave and the PRS is ill-posed. It is more correct to consider the time delay between the rising edge of the PRS and the zero crossing, with positive slope, of the sine wave. Then, it is straightforward to think to employ a frequency counter to measure this time delay. However, the frequency counter, in order to measure the time delay between two signals, adopts trigger circuits to “square” the two waveforms. Especially with low-frequency signals, as in the case here considered, characterized by a low slope in correspondence of the zero crossing, the trigger circuits can introduce an unacceptable uncertainty.

However, it can be analytically demonstrated that the positive zero crossing of the fundamental component of a square wave is coincident with the rising edge of the square wave. Therefore, the problem can be simplified by measuring the phase delay between the sine wave and the fundamental
component of the square wave, through the use of a digital
phase comparator.

The fundamental component of a square wave can be
obtained with a suitable analog filter. However, it is well
known that analog filters introduce noise and could have
problems of time stability, which influences the repeatability
of the measurements. Moreover, their characteristics could be
very sensitive to the environmental conditions.

The phase delay between the sine wave and the PRS
is here measured in the frequency domain, performing the
dFT on the samples of the two waveforms; this is possible
since the considered signals are stationary. As it is known,
the frequency spectral content of a square wave is infinite,
and, thus, the effect of the finite sample rate causes aliasing.
This, in turns, makes some of the aliased high-frequency
components (the harmonic frequencies that differ from a
multiple of the sampling frequency by an amount exactly equal
to the fundamental frequency) sum up to fundamental tone,
cauing the modification of the fundamental phase angle and,
therefore, making the measurement less accurate.

This problem was here solved using a digital antialiasing
filter, with variable order (depending on the chosen sampling
rate) and cutoff frequency equal to about half of the chosen
sampling rate; the filter is internal to the COMP and is
applied to all COMP inputs. In this way, assuming that the
chosen COMP sampling rate is sufficiently higher than the
PRS fundamental frequency (as in this case): 1) the aliasing
problem is prevented; 2) the Nyquist theorem is respected for
the fundamental component of the PRS; and 3) the phase angle
of the fundamental tone of the PRS is correctly evaluated.

Nevertheless, an uncertainty source, due to the fact that
the two input channels of the COMP are stimulated with
waveforms with different characteristics, i.e., a sine wave and
a square wave, has to be considered. In particular, the square
wave could stimulate a residual nonlinear behavior of the
channel, which is not stimulated by the sine wave.

In other words, the hypothesis at the basis of the compensa-
tion of the interchannel phase delay, explained in Section IV-A,
is the linearity of the input channels of the COMP. If signals
that stimulate nonlinear behavior of the channels are used,
then the interchannel phase delay cannot be compensated in
the way it is explained. Nevertheless, two comments are due.

First of all, the used digitizer for the COMP [18] has very
good linearity and noise performances and so its main behavior
can be considered linear. Moreover, even if a residual nonlinear
behavior can be faced when using square waves, it is not a
simplification to assume that the nonlinear behaviors of the
two channels are the same.

If these two hypotheses are true, considering again the
signals in Section IV-A and assuming that the signal \( b \) is the
fundamental component of the PRS, then (10) can be rewritten
as follows:

\[
\begin{align*}
\Delta \phi_1 &= \Delta \phi_{1b} + \Delta \phi_d + \Delta \phi_{1NL} \\
\Delta \phi_2 &= \Delta \phi_{1b} - \Delta \phi_d + \Delta \phi_{2NL}
\end{align*}
\]

where the values \( \Delta \phi_{1NL} \) and \( \Delta \phi_{2NL} \) are the additional phase
displacement due to the square wave when it is applied to the
first and to the second channel, respectively. Since we have
assumed that \( \Delta \phi_{2NL} = \Delta \phi_{1NL} \), then (10) is still valid.

The contributions of these assumptions to the total uncer-
tainty are quantified to be lower than 0.1 \( \mu \)rad at 50 Hz
and 32 \( \mu \)rad at 20 kHz. It has been estimated by measuring
the mismatching between the relative phase error of the two
channels: 1) when they measure the same sine wave and
2) when they measure the same square wave.

D. Uncertainty on Sampling Event of the DUT

Another source of uncertainty is represented by the time
instant in which the DUT that receives a sampling clock pulse
performs the sampling. It is worthwhile noting that, to the aim
of the analyses made in this subsection, the jitter and the noise
of the sampling clock are not considered.

From the datasheet of the DUT [19], it is known that it
recognizes a sampling command when the rising edge of the
sampling clock reaches the value of about 2.2 V.

Therefore, a combined contribution to the total uncertainty
is considered given by: 1) the not perfect vertical rising edge of
the sampling clock and 2) the not perfect recognition of 2.2 V
by the DUT. With the frequency counter, the time interval
between the sampling clock crossings for 2.1 and 2.3 V has
been measured. Its uncertainty contribution has been quantified
to be lower than 10 \( \mu \)rad at 50 Hz and 4 \( \mu \)rad at 20 kHz.

E. Distortions on High-Frequency Content Signals

When a square signal, sampling clock or PRS, is con-
ected to two measuring systems with high input impedance,
as required by the procedure (Fig. 5), a strong distortion arises
at the edge of such signals.

This distortion introduces a high variability in the time delay
measurements. However, no significant distortion has been
detected when the square signal generator is connected to only
one measuring system.

Therefore, under the assumption of good short-term stability
of the generation and acquisition system, the measurements
have been performed in sequence.

F. Uncertainty Budgets

Starting from the analysis of the systematic errors and the
uncertainty sources, shown in Sections IV-A–IV-E, the uncer-
tainty budget is quantified in Table I. It summarizes all the
standard uncertainty contributions, where all the repeatability
and stability contributions are summed up.

<table>
<thead>
<tr>
<th>Source</th>
<th>Frequency [Hz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \phi_T )</td>
<td>0.01</td>
</tr>
<tr>
<td>( \phi_c )</td>
<td>0.2</td>
</tr>
<tr>
<td>( \phi_\rho )</td>
<td>0.1</td>
</tr>
<tr>
<td>Repeatability and stability</td>
<td>1.5</td>
</tr>
</tbody>
</table>

TABLE I
STANDARD UNCERTAINTY CONTRIBUTIONS
V. E XPERIMENTAL RESULTS

The DUT is tested in a variety of conditions. Four different signal amplitudes (1, 2, 5, and 10 V), corresponding to four different DUT input ranges, have been used. Signal frequencies from 1 Hz to 20 kHz have been considered. Two sets of tests have been performed. In the first set, the DUT sampling frequency has been set to 1 MHz and the signal frequency has been varied. In the second set, the signal frequency has been fixed to 50 Hz, whereas DUT sampling frequency has been changed from 1 kHz to 1 MHz.

Tests have been performed for two DUT channels (CH0 and CH1). Here, for the sake of brevity, only the results related to CH0 are shown.

Fig. 8 shows the results of the first set of tests, referring to 1 and 10 V ranges only; the results for 2 V range and 5 V ranges are very similar to those of 10 V range. The inset shows a zoom between 50 and 200 Hz. The performances of the channel slight decrease passing from range 1 V to range 10 V. Fig. 8 shows also the expanded uncertainty (level of confidence 95%). In the considered situation, CH0 exhibits an absolute phase error lower than 10 mrad till 10 kHz. The expanded uncertainty is about 4 μrad at 50 Hz and 150 μrad at 20 kHz.

In Fig. 9, the results of the second set are shown. Also in this case, smaller errors have been found at 1 V, about −43 μrad, with respect to 10 V, about −60 μrad. The behaviors of the other ranges are very similar to each other, with performances slightly lower than those found for the first range. The increase in sampling frequency over a few kilohertz does not produce remarkable improvement in terms of uncertainty. In fact, the expanded uncertainty (level of confidence 95%) is 4 μrad for every sampling frequency.

VI. V ALIDATION WITH PHASE COMPARATOR MEASUREMENTS

In order to demonstrate the validity of the proposed method, an experimental comparison with results obtained by a digital phase comparator was performed.

The relative phase delay between DUT channel 0 and channel 1 has been measured in two different ways: a) as a difference between the absolute phase errors (each measured through the procedure described in Sections II and V) and b) measuring directly their relative phase delay by a previously characterized phase comparator. The same method described in Section IV-A is used to measure the relative phase delay between channel 0 and channel 1 of the DUT. The same signal has been input to channel 0 and channel 1, samples are simultaneously acquired, DFT is applied to the samples and the phase difference of the fundamental components is evaluated. The same two sets of tests discussed in Section V have been performed. Fig. 10 shows the results of the first set of tests, whereas Fig. 11 deals with the results of the second set. Fig. 10 shows also two insets, where the zooms around 50 Hz and around 20 kHz are shown.
The values estimated with the two methods are always in a very good agreement. Maximum deviations are within 2 μrad at 50 Hz and 6 μrad at 20 kHz. The measurement results are always compatible within their uncertainty, considering the correlation due to use of same frequency counter and the PRS. The expanded uncertainty (level of confidence 95%) of the difference of the absolute phase errors is lower than 5 μrad, whereas that of the relative phase error, given by the comparator, is lower than 1.6 μrad up to 20 kHz.

VII. CONCLUSION

In this paper, a method for the measurement of the absolute phase error of a digitizer, defined as the phase displacement between the digitized output and the input analog waveform, is presented. The method is based on the use of a PRS (a square wave), synchronous with the input sine wave, and the characterization of the phase frequency response of the employed AWG. The method has been applied to a high-performance digitizer (10 V, 16 bit, 4 MHz), measuring the absolute phase errors of two different channels. The expanded uncertainty of the method has been quantified as 4 μrad at 50 Hz and 150 μrad at 20 kHz. Good agreement within a few microradians up to 20 kHz has been also found when results of phase differences have been compared with those obtained by a phase comparator.

REFERENCES


Gabriella Crotti received the Laurea degree in physics from the University of Turin, Torino, Italy, in 1986.

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I. INTRODUCTION

The knowledge of phase angles of signals is at the base of many engineering applications, from telecommunications to power systems [1], [2]. In particular, in most measurement applications, electronic instrumentation is based on digitizers to convert analog signals to digital samples that are handled by digital signal processors to get the desired measurement value. However, every digitizer has its own phase frequency response which introduces a phase deviation, between the analog input and its corresponding digital output samples, that is here defined as the absolute phase error of the digitizer. This deviation depends on the characteristics of the digitizer input circuitry and the digitalization architecture. For very low-frequency signals, this phase deviation can be negligible, if the phase displacement reflects into a time delay much lower than the time period of the considered waveform. For many applications, two channels of the same digitizer are involved in the measurement at the same time (i.e., power, energy, or impedance measurement) so that only the relative phase delay between channels is important. Measuring the relative phase delay between the two channels of the same digitizer, or two channels of two different digitizers with synchronized sampling clocks, is an issue faced in a number of scientific papers [3]–[5]. However, there are special applications, such as high-accuracy calibration of Phasor Measurement Units (PMU) for medium voltage grid application [6]–[10] or calibration of low-power instrument transformers [11]–[14] with digital output (DLPT, carried out by comparison with a standard analog transformer), where high phase accuracies, of the order of the microradian, are required. In these situations, the absolute phase deviation of the single channel of the used digitizer may be comparable or higher than the required accuracy, introducing an unacceptable systematic error that highly influences the measurement result.

An interesting technique for the measurement of digitizer absolute phase error was proposed in [15], which involves the generation of a reference signal with known phase with respect to a time reference, but it is not thoroughly discussed and only first results are shown.

In this paper, a different technique for measuring the absolute phase errors of digitizer is presented. The technique has been introduced in [16], but here a thorough theoretical explanation is given, together with an exhaustive uncertainty analysis and an experimental validation. It is based on the preliminary characterization of the phase error of the used analog waveform generator with respect to a phase reference signal (PRS), through the use of a phase comparator [4], [5]. By means of a frequency counter, which measures the time delay between the sampling clock of the digitizer under test (DUT) and the PRS, and applying the discrete Fourier transform (DFT) to the DUT samples, the absolute phase error of the DUT is measured.

This paper is organized as follows. Section II describes the measurement procedure, whereas Section III focuses on the adopted measurement setup. Section IV analyzes systematic errors and uncertainty contributions. Section V discusses the experimental characterization of a digitizing module, and
Section VI, in order to validate the proposed technique, presents a comparison with results obtained through a phase comparator [3]–[5].

II. MEASUREMENT METHOD

The measurement of the absolute phase error of a digitizer involves the evaluation of a phase delay between a digitized quantity, that is the output samples of the digitizer, and an analog quantity (typically a voltage), that is the digitizer input signal. To the best of the authors’ knowledge, direct measurement methods able to quantify this phase error are not available. Therefore, an indirect measurement method, based on the introduction of a reference phase signal (a square wave), having the same frequency of the input signal, has been adopted.

At first, let consider an arbitrary waveform generator (AWG) that also provides a signal that acts as the PRS. This is a square signal with the same periodicity $T_0$ of the generated sinusoidal signal. When a sinusoidal signal $s_g$ is generated, ideally, the zero crossing of the sine wave and square wave should be at the same time instant. Actually, due to the frequency response of the AWG and to its internal time delay, there is a time delay $T_g$ between the zero crossing of sine wave and the rising edge of square wave. Assuming the rising edge of the PRS as the time reference ($t = 0$), the time delay, which corresponds to an initial phase angle of the sine wave equal to $\phi_g$, is

$$\phi_g(f_0) = \frac{2\pi}{T_0} T_g = 2\pi f_0 \cdot T_g = \omega_0 T_g$$

(1)

where $f_0$ is the signal frequency. Thus, the generated sine wave can be written as

$$s_g(t) = \sin(2\pi f_0 t - \phi_g)$$

(2)

where for the sake of simplicity, a unitary amplitude is considered. This effect is illustrated in Fig. 1.

Now, let suppose that PRS is used to trigger the starting of the sampling performed by the digitizer (DUT) to be characterized. Ideally, the first command of the sampling should be aligned with the rising edge of PRS, but, due to the delay of the clock paths, it is actually delayed of a time interval $T_c$ (see Fig. 2).

After that, sampling commands are generated equally spaced of the chosen sampling period $T_s$ with the accuracy of the adopted sampling clock (Fig. 2).

In a digitizer, the sampling command should ideally produce an instantaneous acquisition of a sample but, actually, there is always a delay $T_d$ between the sampling command and the acquisition of the sampled value. This delay impacts on the acquired waveform as a phase shift. This, summed to the phase shift $\phi_{a\text{ DUT}}$ introduced by the transfer function of the analog input circuitry of the digitizer, determines a phase error, i.e., the absolute phase error of the digitizer ($\phi_{\text{DUT}}$). Therefore, the absolute phase error of the DUT can be expressed as

$$\phi_{\text{DUT}} = 2\pi f_0 T_d + \phi_{a\text{ DUT}}.$$  

(3)

As a consequence, the time delay between the sampling command and the acquisition of the sampled value is

$$T_{\text{DUT}} = \frac{\phi_{\text{DUT}}}{2\pi f_0}.$$  

(4)

This situation is depicted in Fig. 3.

In order to evaluate the absolute phase error, let suppose that the DUT is supplied with a signal $s_g$ and the PRS triggers...
the sampling performed by the DUT. All the phenomena
previously shown occur together, as shown in Fig. 4.

The sinusoidal waveform acquired by the DUT can be
expressed as
\[
\varphi_{\text{DUT}}(kT_s) = \sin(2\pi f_0(kT_c + T_c - T_D - T_T)) \\
= \sin(2\pi f_0kT_c + \varphi_c + \varphi_D - \varphi_G) \\
= \sin(2\pi f_0kT_c + \varphi_T) \\
\]  
(5)

where time delays are given in terms of phase displace-
ments (1). The term \(\varphi_T\) represents the comprehensive effect
of all the time delays on the phase displacement of the
acquired sinusoid. The phase angle \(\varphi_T\) can be evaluated by
performing the DFT on the acquired samples and evaluating
the phase angle at frequency \(f_0\) with a synchronized acquisi-
tion or different signal processing techniques. The phase
deviation \(\varphi_D\), introduced by the DUT at frequency \(f_0\), can
be then obtained by
\[
\varphi_D = \varphi_T - \varphi_c + \varphi_G \\
\]  
(6)

where the phase delays \(\varphi_c\) and \(\varphi_G\) are measured as detailed in
the following.

III. MEASUREMENT SETUP

To validate the proposed method, a proper automated test
bench has been realized. Its block scheme is shown in Fig. 5.

The system is based on a PXI (PCI eXtension for Instru-
mentation) chassis: a GPS-disciplined Rubidium atomic clock
(Fluke 910R) and an external universal frequency counter
(Agilent 53230A). The multifunction I/O module National
Instruments (NI) PXIe-6124 (±10 V, 16 bit, maximum sam-
ping rate 4 MHz) is the DUT. The module NI PXI-5422
(±12 V, programmable gain, 16 bit, maximum sampling rate
200 MHz) has been used for AWG. The NI PXI 4462 (±10 V,
24 bit, maximum sampling rate of 204.8 kHz) module is used
as a phase comparator.

All the instruments of the test bench operate synchronously
since the clock source from the Fluke 910R is provided to
the whole PXI backplane and to the frequency counter
as external time base. Clock signals (with frequency dif-
f erent from 10 MHz) and trigger signals are generated by
the NI PXI-6683H synchronization board. In particular, the
sampling clock of DUT \(C_{\text{DUT}}\) (Fig. 5), the PRS and the
AWG generation clock \(C_{\text{AWG}}\) in Fig. 5, set to 5 MHz) are
generated by the NI PXI-6683H. A digital storage oscilloscope
(Lecroy MDA810, not shown in Fig. 5) is used to control the
correct operation of the setup and measure the rise time of
the PRS. It is worth to underline that \(C_{\text{DUT}}\) is externally pro-
vided to the DUT, through the terminal PF10 (Programmable
Function Input 0); moreover, the DUT starts to sample when it
recognizes the first pulse of the sample clock, which is delayed
from PRS of a time \(T_c\) (see Fig. 2).

The AWG, generating the sine wave \(s_g\), is connected to
both the DUT and phase comparator (COMP), which measures
the phase difference \(\varphi_g\) between \(s_g\) and PRS. The frequency
counter gives the time delay \(T_c\) between PRS and DUT
sampling clock. All the clock and signal paths are symmetrically
managed (as better explained in the following) in order to
avoid different propagation delays.

Measurement software is developed in LabVIEW, using the
event-based state-machine approach.

For each test point, amplitude and frequency of the test sig-
nal of the DUT can be chosen and 30 repeated measurements
of \(\varphi_T\), \(T_c\), and \(\varphi_G\) are performed. In order to evaluate \(\varphi_T\),
for each test frequency, a time window equal to a fixed number
of signal periods is used to perform the DFT.

For the sake of simplicity, in the realized setup, a DUT
which accepts external sampling clock is used. However,
the proposed method does not lose generality even in the
presence of a DUT which accepts the sampling clock through
the communication bus (whatever it is), since it is sufficient
to access to the pin receiving the sampling clock.

IV. SYSTEMATIC ERRORS AND SOURCES
OF UNCERTAINTY

A. Counter and Comparator Interchannel Delay

Both the measurement values given by the phase com-
parator, \(\varphi_g\), and the frequency counter, \(T_c\), are affected by
systematic errors due to differential time delay between the
two paths to the channel inputs of the instruments. These
systematic effects can be estimated and corrected as briefly
described in the following.

Let consider the two input paths of a frequency counter,
as depicted in Fig. 6(a): \(T'_a\) and \(T'_b\) indicate the time delays
in propagation due to the cables that connect the signals
Similar considerations can be done for the phase comparator, considering now that the signals at its inputs have relative phase delay of $\Delta \phi_{d}$. The introduced uncertainty contribution depends on the repeatability and stability of the generated signals. In this case, the systematic effect introduced by the comparator can be modeled with a differential phase displacement $\Delta \phi_{ab}$.

Performing two measurements, inverting the inputs, (10) is obtained. It results

$$
\begin{align*}
\Delta \phi_1 &= \Delta \phi_{ab} + \Delta \phi_d \\
\Delta \phi_2 &= \Delta \phi_{ab} - \Delta \phi_d
\end{align*}
$$

### B. Time Delay Between DUT Sampling Clock and PRS

As it is explained in Section II, the rising edge of the PRS is considered as the time reference ($t = 0$), and, thus, all the measured time or phase delays are referred to it. However, an uncertainty source has to be considered as associated with this assumption that is the fact that the PRS is not an ideal square wave; this aspect particularly affects the measurement of the time delay between the DUT sampling clock and the PRS. In fact, the intrinsic low-pass behavior of the PRS generation affects amplitudes and phases of all harmonic components of the generated square wave, possibly introducing phase delays. Nevertheless, if the analog bandwidth of the PRS generator is sufficiently greater than the fundamental frequency of the generated square wave, then the contribution to the total uncertainty, due to this assumption, can be considered small. For the case at hand, the square waves (PRS and DUT sampling clock) are generated by the synchronization board, which is optimized to deal with square waves and has an analog bandwidth of about 50 MHz, whereas the maximum analyzed frequency is 20 kHz, that is more than three orders of magnitudes lowers. However, measuring the rise time of the PRS, the estimated uncertainty contribution is lower than 0.2 $\mu$rad at 50 Hz and 68 $\mu$rad at 20 kHz.

### C. Phase Delay Between Sine Wave and PRS

From a mathematical point of view, the phase is defined for a sine wave with respect to a time reference. Therefore, the problem of measuring the phase delay between the sine wave and the PRS is ill-posed. It is more correct to consider the phase delay between the rising edge of the PRS and the zero crossing, with positive slope, of the sine wave. Then, it is straightforward to think to employ a frequency counter to measure this time delay. However, the frequency counter, in order to measure the time delay between two signals, adopts trigger circuits to “square” the two waveforms. Especially with low-frequency signals, as in the case here considered, characterized by a low slope in correspondence of the zero crossing, the trigger circuits can introduce an unacceptable uncertainty.

However, it can be analytically demonstrated that the positive zero crossing of the fundamental component of a square wave is coincident with the rising edge of the square wave. Therefore, the problem can be simplified by measuring the phase delay between the sine wave and the fundamental

$$
\tau_d = \frac{\Delta T_1 + \Delta T_2}{2}.
$$

In this way, performing two measurements and combining opportunely the results, the systematic time delay between channel A and channel B is automatically compensated.
component of the square wave, through the use of a digital phase comparator.

The fundamental component of a square wave can be obtained with a suitable analog filter. However, it is well known that analog filters introduce noise and could have problems of time stability, which influences the repeatability of the measurements. Moreover, their characteristics could be very sensitive to the environmental conditions.

The phase delay between the sine wave and the PRS is here measured in the frequency domain, performing the DFT on the samples of the two waveforms; this is possible since the considered signals are stationary. As it is known, the frequency spectral content of a square wave is infinite, and, thus, the effect of the finite sample rate causes aliasing. This, in turns, makes some of the aliased high-frequency components (the harmonic frequencies that differ from a multiple of the sampling frequency by an amount exactly equal to the fundamental frequency) sum up to fundamental tone, causing the modification of the fundamental phase angle and, therefore, making the measurement less accurate.

This problem was here solved using a digital antialiasing filter, with variable order (depending on the chosen sampling rate) and cutoff frequency equal to about half of the chosen sampling rate; the filter is internal to the COMP and is applied to all COMP inputs. In this way, assuming that the chosen COMP sampling rate is sufficiently higher than the PRS fundamental frequency (as in this case): 1) the aliasing problem is prevented; 2) the Nyquist theorem is respected for the fundamental component of the PRS; and 3) the phase angle of the fundamental tone of the PRS is correctly evaluated.

Nevertheless, an uncertainty source, due to the fact that the two input channels of the COMP are stimulated with waveforms with different characteristics, i.e., a sine wave and a square wave, has to be considered. In particular, the square wave could stimulate a residual nonlinear behavior of the channel, which is not stimulated by the sine wave.

In other words, the hypothesis at the basis of the compensation of the interchannel phase delay, explained in Section IV-A, is the linearity of the input channels of the COMP. If signals that stimulate nonlinear behavior of the channels are used, then the interchannel phase delay cannot be compensated in the way it is explained. Nevertheless, two comments are due.

First of all, the used digitizer for the COMP [18] has very good linearity and noise performances and so its main behavior can be considered linear. Moreover, even if a residual nonlinear behavior can be faced when using square waves, it is not a simplification to assume that the nonlinear behaviors of the two channels are the same.

If these two hypotheses are true, considering again the signals in Section IV-A and assuming that the signal \( b \) is the fundamental component of the PRS, then (10) can be rewritten as follows:

\[
\begin{align*}
\Delta \phi_1 &= \Delta \phi_{ab} + \Delta \phi_d + \Delta \phi_{1,NL} \\
\Delta \phi_2 &= \Delta \phi_{ab} - \Delta \phi_d + \Delta \phi_{2,NL}
\end{align*}
\]

(11)

where the values \( \Delta \phi_{1,NL} \) and \( \Delta \phi_{2,NL} \) are the additional phase displacement due to the square wave when it is applied to the first and to the second channel, respectively. Since we have assumed that \( \Delta \phi_{2,NL} = \Delta \phi_{1,NL} \), then (10) is still valid.

The contributions of these assumptions to the total uncertainty are quantified to be lower than 0.1 \( \mu \text{rad} \) at 50 Hz and 32 \( \mu \text{rad} \) at 20 kHz. It has been estimated by measuring the mismatching between the relative phase error of the two channels: 1) when they measure the same sine wave and 2) when they measure the same square wave.

### D. Uncertainty on Sampling Event of the DUT

Another source of uncertainty is represented by the time instant in which the DUT that receives a sampling clock pulse performs the sampling. It is worthwhile noting that, to the aim of the analyses made in this subsection, the jitter and the noise of the sampling clock are not considered.

From the datasheet of the DUT [19], it is known that it recognizes a sampling command when the rising edge of the sampling clock reaches the value of about 2.2 V.

Therefore, a combined contribution to the total uncertainty is considered given by: 1) the not perfect vertical rising edge of the sampling clock and 2) the not perfect recognition of 2.2 V by the DUT. With the frequency counter, the time interval between the sampling clock crossings for 2.1 and 2.3 V has been measured. Its uncertainty contribution has been quantified to be lower than 10 nrad at 50 Hz and 4 \( \mu \text{rad} \) at 20 kHz.

### E. Distortions on High-Frequency Content Signals

When a square signal, sampling clock or PRS, is connected to two measuring systems with high input impedance, as required by the procedure (Fig. 5), a strong distortion arises at the edge of such signals.

This distortion introduces a high variability in the time delay measurements. However, no significant distortion has been detected when the square signal generator is connected to only one measuring system.

Therefore, under the assumption of good short-term stability of the generation and acquisition system, the measurements have been performed in sequence.

### F. Uncertainty Budgets

Starting from the analysis of the systematic errors and the uncertainty sources, shown in Sections IV-A–IV-E, the uncertainty budget is quantified in Table I. It summarizes all the standard uncertainty contributions, where all the repeatability and stability contributions are summed up.

### Table I

<table>
<thead>
<tr>
<th>Source</th>
<th>Frequency [Hz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \varphi_T )</td>
<td>0.01</td>
</tr>
<tr>
<td>( \varphi_c )</td>
<td>0.2</td>
</tr>
<tr>
<td>( \varphi_d )</td>
<td>0.1</td>
</tr>
<tr>
<td>Repeatability and stability</td>
<td>1.5</td>
</tr>
</tbody>
</table>

This problem was here solved using a digital antialiasing filter, with variable order (depending on the chosen sampling rate) and cutoff frequency equal to about half of the chosen
V. EXPERIMENTAL RESULTS

The DUT is tested in a variety of conditions. Four different signal amplitudes (1, 2, 5, and 10 V), corresponding to four different DUT input ranges, have been used.

Signal frequencies from 1 Hz to 20 kHz have been considered. Two sets of tests have been performed. In the first set, the DUT sampling frequency has been set to 1 MHz and the signal frequency has been varied.

In the second set, the signal frequency has been fixed to 50 Hz, whereas DUT sampling frequency has been changed from 1 kHz to 1 MHz.

Tests have been performed for two DUT channels (CH0 and CH1). Here, for the sake of brevity, only the results related to CH0 are shown.

Fig. 8 shows the results of the first set of tests, referring to 1 and 10 V ranges only; the results for 2 V range and 5 V ranges are very similar to those of 10 V range. The inset shows a zoom between 50 and 200 Hz. The performances of the channel slight decrease passing from range 1 V to range 10 V. Fig. 8 shows also the expanded uncertainty (level of confidence 95%). In the considered situation, CH0 exhibits an absolute phase error lower than 10 mrad till 10 kHz. The expanded uncertainty is about 4 μrad at 50 Hz and 150 μrad at 20 kHz.

In Fig. 9, the results of the second set are shown. Also in this case, smaller errors have been found at 1 V, about −43 μrad, with respect to 10 V, about −60 μrad. The behaviors of the other ranges are very similar to each other, with performances slightly lower than those found for the first range. The increase in sampling frequency over a few kilohertz does not produce remarkable improvement in terms of uncertainty. In fact, the expanded uncertainty (level of confidence 95%) is 4 μrad for every sampling frequency.

VI. VALIDATION WITH PHASE COMPARATOR MEASUREMENTS

In order to demonstrate the validity of the proposed method, an experimental comparison with results obtained by a digital phase comparator was performed.

The relative phase delay between DUT channel 0 and channel 1 has been measured in two different ways: a) as a difference between the absolute phase errors (each measured through the procedure described in Sections II and V) and b) measuring directly their relative phase delay by a previously characterized phase comparator. The same method described in Section IV-A is used to measure the relative phase delay between channel 0 and channel 1 of the DUT. The same signal has been input to channel 0 and channel 1, samples are simultaneously acquired, DFT is applied to the samples and the phase difference of the fundamental components is evaluated. The same two sets of tests discussed in Section V have been performed. Fig. 10 shows the results of the first set of tests, whereas Fig. 11 deals with the results of the second set. Fig. 10 shows also two insets, where the zooms around 50 Hz and around 20 kHz are shown.
The values estimated with the two methods are always in a very good agreement. Maximum deviations are within 2 μrad at 50 Hz and 6 μrad at 20 kHz. The measurement results are always compatible within their uncertainty, considering the correlation due to use of same frequency counter and the PRS. The expanded uncertainty (level of confidence 95%) of the difference of the absolute phase errors is lower than 5 μrad, whereas that of the relative phase error, given by the comparator, is lower than 1.6 μrad up to 20 kHz.

VII. CONCLUSION
In this paper, a method for the measurement of the absolute phase error of a digitizer, defined as the phase displacement between the digitized output and the input analog waveform, is presented. The method is based on the use of a PRS (a square wave), synchronous with the input sine wave, and the characterization of the phase frequency response of the employed AWG. The method has been applied to a high-performance digitizer (10 V, 16 bit, 4 MHz), measuring the absolute phase errors of two different channels. The expanded uncertainty of the method has been quantified as 4 μrad at 50 Hz and 150 μrad at 20 kHz. Good agreement within a few microradians up to 20 kHz has been also found when results of phase differences have been compared with those obtained by a phase comparator.

REFERENCES

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