1 kV Wideband Voltage Transducer, a Novel Method for Calibration and a Voltage Measurement Chain

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***Abstract*— A new reference resistive-capacitive voltage divider is presented in this paper, operating in dc and ac from 10 to 200 kHz. The ratio error is lower than 0.1% and the phase error is lower than 400 μrad (1.375') at 100 kHz. The divider is stable and repeatable. The scale factor (SF) and the phase error repeatability, tested in 24-h continuous measurements repeated during 15 weeks, show an SF variation lower than 80 ppm and a phase error variation lower than 20 μrad. This allows one to define a calibration matrix of the device bringing its relative measurement uncertainty lower than $0.5 \cdot 10^{-3}$. The divider calibration has been obtained with a step-up method, which could improve traceability in many laboratories and is described in this paper. The divider can be embedded in a calibration chain to test the accuracy of voltage transducers in the measurement of the ac voltage ripple, in the presence of a significant dc component, as it occurs in many power electronic systems. The voltage calibration chain is based on the use of the reference divider and a voltage injector, the secondary of which is placed in series with a stable dc source. By means of this calibration system, one of the best commercial voltage transducers on the market has been analyzed. This paper also highlights how the proposed voltage calibration chain could be used in perspective in a phantom power system for the development of a dc plus ac power standard.**

***Index Terms*— Calibration, electric vehicles (EVs), measurement techniques, measurement uncertainty, voltage measurement.**

I. Introduction

ACCURATE power and efficiency measurements are very important for electric automotive applications and design. High-accuracy voltage measurements become critical when frequency bandwidth and voltage magnitude increase, since many commercially available probes show low accuracy, especially at increasing frequency [1]. Applications with higher voltage harmonics (some hundreds of volts up to 1 kV) such as electric drives and inductive power transfer (IPT) are likely to increase in a near future, which ask for accurate voltage transducers with a higher frequency bandwidth. For instance, in high-power IPT applications, full-bridge inverter consisting of IGBT or MOSFET switches is frequently used for its high-power capacity, ideally producing square wave voltage containing a large amount of harmonics [1]. Besides the implementation of such transducers, there is also the need for their calibration, which is a non-negligible task when high frequency is together with voltages of the order of 1 kV or, at any rate, hundreds of volts.

The IPT for vehicles charging is an electrical automotive application of growing interest. IPT occurs between two coils through the coupling of a magnetic field; the first coil (transmitter) located a few centimeters below the asphalt, which is at about ground level, and the second (receiver) placed on board the vehicle. Each coil is connected to its own resonant circuit, and both circuits resonates at the same frequency, which can vary from 20 to over 100 kHz, being a typical resonance frequency equal to 85 kHz [2], [3]. An ac–dc converter then rectifies the coil signal induced on board; the voltage to be measured at the battery being charged is a dc signal with the superposition of a non-negligible periodic ripple that is induced by converters.

As in the inductive charging, the accurate voltage measurement is difficult to be obtained nowadays, with the commercially available instrumentation. To this reason, some authors have tried to develop alternative measuring devices. Grubmüller *et al*. [4] developed an interesting differential voltage probe with wide and flat frequency response compared to commercial probes, which shows a ratio error of about $\pm 0.1\%$ up to 1 kHz and $\pm 0.2\%$ up to 2 MHz. However, few evidences are provided concerning repeatability and stability of the results; moreover, the results related to phase error are not readable in detail. In [5], a high accuracy resistive voltage divider (VD) from 400 Hz to 100 kHz and having ratios of 100 and 200 is presented. However, the maximum voltage is limited to about 100 V, and the low impedance seen by the input voltage makes the power consumption and the heating effect not negligible.

This paper develops a preliminary investigation shown in [6] and proposes a laboratory facility, suited to perform the calibration of sensor probes for voltage measurement in electric drive and electric vehicle (EV) systems. Then, this paper shows the design, the realization, and the characterization of a reference resistive-capacitive divider having target relative

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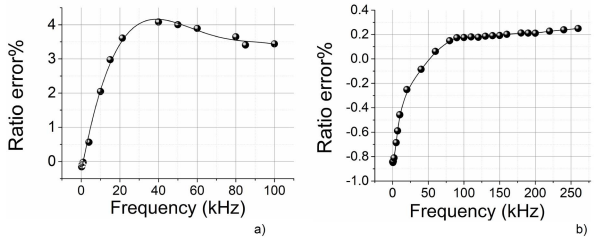

Fig. 1. Percentage ratio error of the two differential probes under test. (a) First commercial meter probe. (b) Second commercial meter probe.

uncertainty of $0.5 \cdot 10^{-3}$. The laboratory facility includes two systems for generating the voltage signal up to 1 kV. A voltage calibrator generates dc voltages. An ac ripple up to 200 kHz is produced by a signal generator and an amplifier and is added to the measurement circuit through a voltage injector able to transfer up to ∼150 V ac peak in the voltage chain. The facility includes the measurement section, which comprises the reference voltage transducer.

This paper also shows an original calibration procedure for the characterization of the reference VD. Such a procedure is suitable for voltage over 1 kV and some hundreds of kilohertz. This could be interesting in order to improve calibration capabilities also at National Metrological Institutes, since calibration capabilities are currently limited to about 100 V and 100 kHz.

This paper is organized as follows. Section II discusses the preliminary results about commercial probes. Section III discusses the proposed calibration circuit and components. Section III-A discusses the voltage calibration circuit, tuning, of the voltage chain and how the circuit could be included in a power calibration facility. Section III-B discusses the voltage injector. Section III-C discusses the VD and design criteria. Section IV discusses the proposed novel method for the calibration of the reference VD and results. Section V discusses the results of the calibration of two identical probes carried out with the circuit described in Section III. The results are summarized and discussed in Section VI.

II. Performances of Commercial Voltage Probes

As a first step, the frequency performances of commercial differential active voltage probes used for measurement in EV technology development were investigated. The ratio error was preliminary obtained by comparing the applied voltage measured by a Keysight 3458A multimeter with the probe output measured by an oscilloscope. The rated specifications of the considered probes were: bandwidth 20 MHz, differential voltage 1400 V_{pk}, best low-frequency accuracy 1% of reading. Fig. 1 shows the measured ratio error where an ac ripple having magnitude of 282 V peak to peak has been applied to the probes. It can be noted how the rated accuracy is found only in dc for the first probe, whereas for the second one, only at power frequency. In the frequency range of interest for electrical drives and IPT, in particular (20–150 kHz plus dc), the ratio error varies from 2.5% to 4.2% for the first probe considered and is about 0.2% for the second,

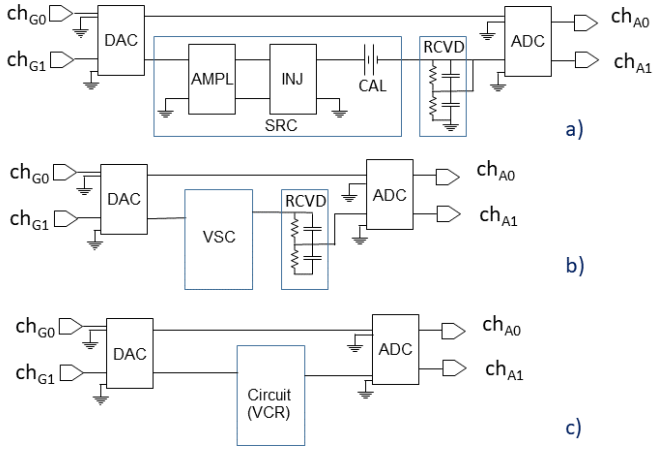

Fig. 2. Same voltage chain circuit in three different representations. (a) DAC: digital to analog converter, AMPL: ac amplifier, INJ: voltage injector, CAL: dc voltage calibrator, RCVD: resistive capacitive reference VD, and ADC: analog-to-digital converter (Card NI PXI 5922). (b) VSC: voltage supply chain. (c) VCR: complete voltage circuit.

while the latter has a ratio error of −0.8% in dc. As also pointed out in [4], it is, therefore, difficult to obtain accurate voltage measurements with commercial meters, and therefore new broadband meters, as the one proposed in this paper, are necessary. Moreover, when the voltage measurement is associated with a power measurement also the phase error is important. This has been measured with the calibration circuit proposed in Section IV-A. For more results about the probe shown in Fig. 1(b), see Section V.

III. Calibration Circuit

A. Architecture, Circuit, Components, and Tuning

Fig. 2 shows the scheme of the voltage calibration circuit. It consists of two channels (ch_{G0} and ch_{G1}) generation card (NI PXIe-5433), which has been chosen for its ability to reproduce complex high-frequency waveforms. One channel of this card is connected to a voltage calibrator, which provides a stable dc voltage. Series connected to the calibrator, a voltage injector designed for the purpose is included in the circuit, supplied by an ac amplifier (NF Model HSA-4052) driven by a signal generator. The voltage injector is a wideband transformer, which is obtained by a proper core and two windings with the same number of turns. Its function is to add the ac signal up to 400 V_{pk-pk} to the dc voltage, keeping the galvanic isolation between the ac and the dc generators. The total voltage is generated by the group including ac amplifier, injector, and dc calibrator; for brevity, this group is called voltage supply chain (VSC) in the following (see Fig. 2). The voltage produced by the VSC is measured through a reference resistive-capacitive VD (RCVD) by two channels (ch_{A0} and ch_{A1}) oscilloscope card (NI PXI-5922). The VSC including the measurement transducer (RCVD) is called "complete voltage circuit" (VCR) in the following (see Fig. 2).

The voltage measurement chain could be used in the development of a dc + ac power standard, based on a phantom power, such as the one shown in Fig. 3(a),

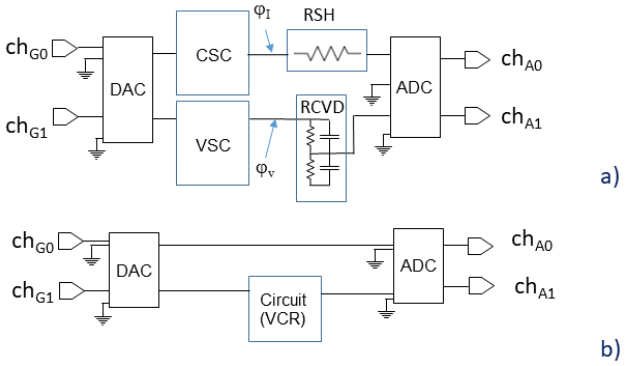

Fig. 3. (a) Representation of a phantom power, including the VSC, the voltage transducer (RCVD), CSC, and the RSH. (b) Schematic of voltage chain calibration.

following the idea proposed in [7]. The current chain should be similar to the voltage chain including the current source circuit (CSC) and the reference current shunt (RSH). Here, the two voltage and current chains combine themselves to simulate a virtual power even though they are two distinct circuits and not electrically connected. Due to synchronization reasons, they have the signal generation and the acquisition cards in common.

What is important is to generate a known phase difference between the input of the voltage and current transducer. To do this, there are several possible approaches. One approach, based on a separate tuning of the voltage and current circuits is proposed in Appendix A. The authors succeeded in setting the phase of the voltage with an accuracy close to 0.02° (350 μrad).

B. Voltage Injector

The voltage injector is a wideband transformer, which is obtained by a proper core and two windings having the same number of turns, to have almost the same voltage both at the output and at the input. The core has been made of nanocrystalline material (Vitroperm 500), whose relative magnetic permeability varies almost linearly in the logarithmic scale from $\mu_r \approx 80\,000$ at 20 kHz up to $\mu_r \approx 8000$ at 1 MHz. Such a behavior allowed an easy estimation of the winding inductances versus frequency.

Fixing the operating voltage (200 V peak) and the device frequency bandwidth (20–200 kHz) as constraints, the injector design has been carried out minimizing the ratio and phase errors. Two available core geometries and different turn numbers have been considered in order to find a good compromise between the accuracy of the ratio and the required bandwidth. Then, having established the geometry of the core (W424 from Vacuumschmelze, saturation induction 1.2 T), the number of turns has been determined equal to 20 for both windings. The transformer frequency performances were estimated using the T-circuit as a representation, and Mathcad as a tool for simulations. The network of stray capacitances between the winding turns has been taken into account and the injector scheme and its final parameters are derived for the circuit shown in Fig. 4 and reported in Table 1, respectively. From the simulation by the model, such design guarantees a flat

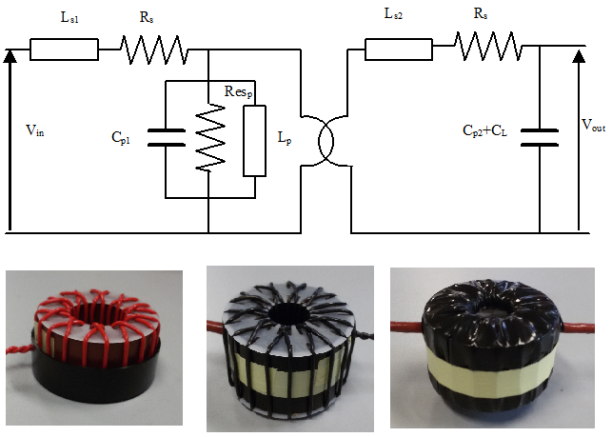

Fig. 4. Circuital representation of the voltage injector and images of its realization.

TABLE I
COMPUTED PARAMETERS OF THE INJECTOR

Parameter	Value	Parameter	*Value*
Core	VAC W424	R_{ESp}	10.11 kΩ
Turns	20 in two layers	R_{s1}	0.118 Ω
$L_{p\,(20\,kHz)}$	33.7 mH	R_{s2}	0.153 Ω
$L_{p\,(1\,MHz)}$	3.37 mH	C_{p1}	36.65 pF
L_{s1}	0.795 µH	C_{p2}	39.32 pF
L_{s2}	1.26 µH		

TABLE II
MEASURED PARAMETERS OF THE INJECTOR AT 100 KHZ

Parameter	Rated Value	Measured
$L_{s1}+L_{s1}$	2.055 µH	2.52 µH
$R_{s1}+R_{s2}$	0.271 Ω	0.227 Ω
R_{ESp}	10.11 kΩ	10.72 kΩ

response of the injector up to more than 150 kHz, covering the bandwidth for the considered application.

As shown in Fig. 4, each winding is made of two layers to avoid the concatenation of residual transversal turns [8] and particular care has been devoted to the insulation between the windings to sustain the dc voltage difference (up to 1 kV).

The injector has been tested to show the compliance to the limits (dc voltage up to 1200 V between the primary and secondary windings and 250 V peak ac voltage at 20 kHz applied to the primary winding) and some intrinsic parameters have been measured as a design verification (see Table II).

Using the method described in Appendix C and derived from Section IV procedure, the ratio error and the phase difference introduced by the injector have been measured and reported in Appendix C. The measurement has shown a ratio error of about 20 μV/V, 0.5 mV/V, and 2 mV/V at 30, 100 and 200 kHz, respectively, and a phase difference of 16, 80, and 210 μrad at 30, 100, and 200 kHz, respectively.

C. Reference Divider Design Criteria and Realization

Applications to IPT in the vehicle charging show applied voltages in the resonant and in the charging circuit lower than 1 kV [9]–[12]. This is why 1 kV has been chosen as the voltage upper limit for the VD under design for IPT applications.

Design steps, details, and modeling tool including finite-element calculations of the divider stray capacitances are provided in [13]. In the following, the authors will describe mainly the project criteria.

As a preliminary remark, in the following, the part of the divider connected to the input will be called "high voltage" (HV) section, whereas the part placed between output and ground will be called "low voltage" (LV) section.

Since the reference divider frequency bandwidth is higher than 5 kHz, the HV resistor and capacitor are chosen in a way to have a cutoff frequency lower than this value. It is well known that keeping constant the capacitance, the bigger the value of the resistor the lower is the cutoff frequency of the VD, being related to $1/(R_{\mathrm{HV}} \cdot C_{\mathrm{HV}})$, where R_{HV} and C_{HV} are the resistance and the capacitance values of the HV section components of the divider, respectively. Furthermore, a larger value for the HV resistor makes the power dissipation of the VD lower.

The nominal scale factor (SF) of the VD is a design parameter and was set to ∼200 for the considered divider, in order to set the maximum 1 kV input to 5 V, this latter compatible with the majority of acquisition cards.

Keeping constant the SF, increasing the value of the HV resistor the value of the LV resistor should be also increased, which rises the dependence of the VD to the load (input impedance of the connected meter). This is why a tradeoff should be considered while selecting the HV components.

As the authors have previously experienced [14], [15], it is advisable to choose the resistors so that they use only a fraction of their rated power during operation, making the heating effect negligible. This is because of their nonlinear behavior increasing temperature; consequently, in the VD design, an HV resistor with 2 W rated power has been implemented, while the maximum considered power dissipation is about 50 mW.

As discussed in [14] and [15], there are two main different kinds of stray capacitances inside a VD that act differently. The stray capacitance between the conductive part of the VD and the ground is called capacitance versus ground (CG), whereas the stray capacitance between the conductive parts of the HV section toward each other, excluding ground, is called CHV. To have the best possible frequency behavior with the minimum possible ratio and phase error, CHVs and CGs should be balanced [14]. The process of balancing stray capacitances depends on many parameters such as distances between conductors and their length, size inside the VD, properties of the insulation supports, and so forth. The optimization of such apparatus having many degrees of freedom has been done by an FEM approach for the calculation of the stray capacitances. Then, a MATLAB program has been utilized to simulate the equivalent circuit of the divider and to compute its frequency response [13].

A preliminary dimensioning was carried out, assuming the realistic dimensions of the components (resistors and capacitors) and choosing a conductive cylindrical shaped encasing. For the latter, high-conductivity copper has been chosen, so that to have the VD shielded, in order to avoid external noise and to make the proximity effect negligible.

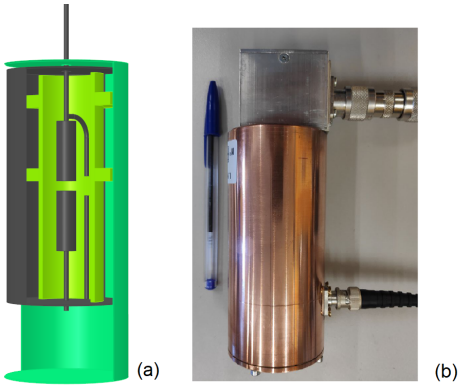

Fig. 5. RCVD (a) model and (b) its final implementation (the outer screen is ground connected).

Then, an HV 20 MΩ resistor has been chosen and stray capacitances have been calculated consequently through the FEM model. All of stray capacitances are less than 0.5 pF inside the HV section. Next, a 3 kV 200 pF capacitor is added in parallel to the HV resistor, in order to decrease the effect of stray capacitances. A larger value for the HV capacitor decreases the value of the impedance of the reference divider at higher frequencies increasing the absorbed current, which should be avoided.

Finally, a set of paralleled capacitors (∼40 nF) has been placed in the output of the VD in order to have a balanced ratio between the CHVs and CGs.

The final design of the RCVD is shown Fig. 5(a). As can be noted, an additional shield has been inserted in the RCVD design, which is able to shield the HV section (both resistor and capacitor). Such a shield is connected to the output terminal of the VD introducing the LV potential around the HV section. The HV components are isolated from the LV shield by means of a shell made of Delrin. The LV-connected screen is inside the bigger ground-connected one (the external case) that shields the whole RCVD, which is shown as realized in Fig. 5(b).

IV. Calibration of the Voltage Divider

A. Step-Up Procedure

The proposed new calibration procedure has been developed considering similar procedures commonly used in the field of ac–dc transfer standards. For instance, a similar procedure has been applied by one of the authors to a resistive VD [16], [17]. However, as far as the authors know, there is not a complete work on the step-up procedure, in this frequency and voltage ranges, using capacitive dividers and determining equations for ratio and phase error.

To implement such a method, two additional auxiliary dividers made with stable capacitors are needed: a capacitive VD (CVD1 in the following) having an SF ∼10 and a second capacitive VD (CVD2 in the following) having a ratio ∼100. The scheme and implementation of the two dividers are shown in Fig. 6.

To apply the procedure, a generation and an acquisition card are needed, together with a voltage amplifier. For the purpose, the same components presented in Section III-A are suitable,

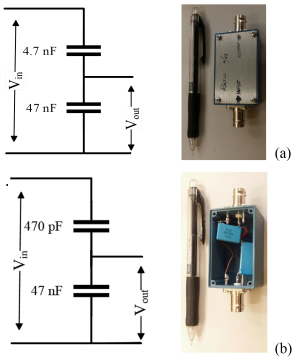

Fig. 6. Circuit of (a) CVD1 and (b) CVD2 (the cap shielding the CVD2 is removed so as to show the internal section).

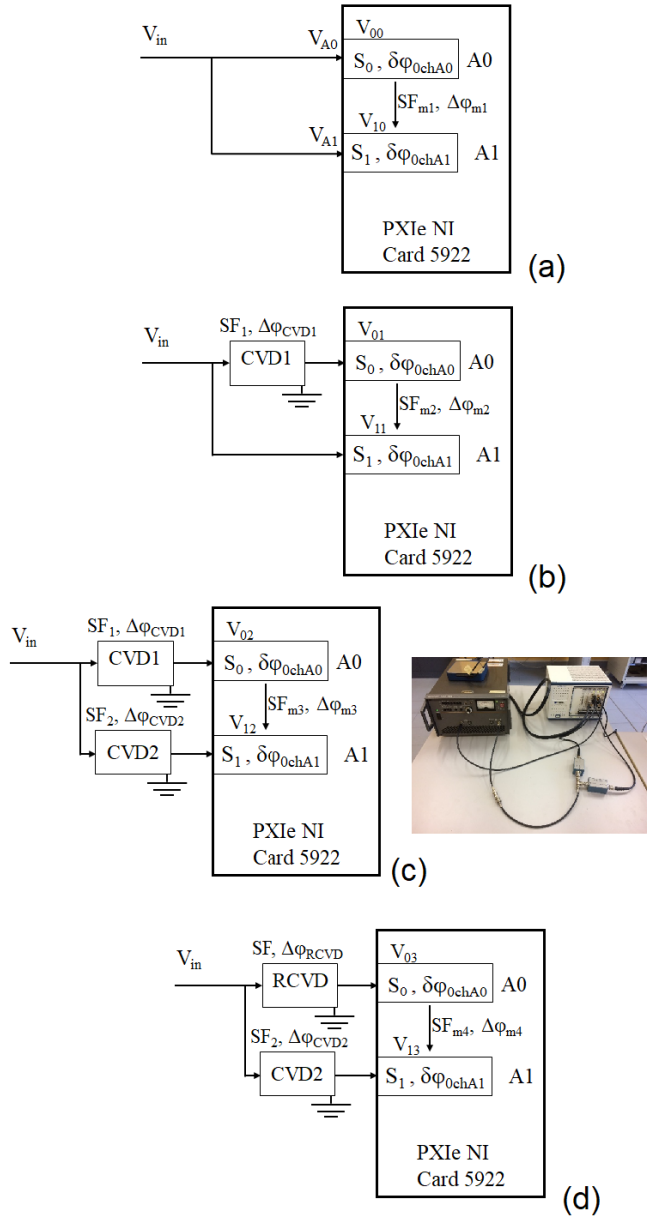

Fig. 7. Circuital setup for the SF characterization. (a) First step. (b) Second step. (c) Third step. (d) Fourth step.

that is, a generation card NI PXIe 5433, an acquisition card NI PXI 5922, and a voltage amplifier NF HSA-4052. The calibration procedure is shown in Fig. 7.

In [18], when the frequency response of the transducer can be proven not to be affected by the amplitude of the fundamental voltage and varying burden (input impedance of the connected meter), the frequency response test can be performed at a voltage level lower than the rated voltage by applying a single tone sine wave and varying the frequency. The test on the RCVD has been repeated for five single tones, choosing as input ac voltages values in the range from 20 to about 160 V.

The quantities in the following, like phase shifts $\delta\varphi$ or SF are, in principle, function of the signal amplitude and frequency as $\delta\varphi = \delta\varphi(\text{ampl}, f)$ and $\text{SF} = \text{SF}(\text{ampl}, f)$. The authors verified that using the NI PXI 5922 board as analog-to-digital converter (ADC), there is no significant dependence of phase shift from the amplitude, but only from the frequency. For the sake of simplicity, such a dependence is omitted in the next paragraphs, but all the tests in the following have been performed at 20 different frequency values, from 10 to 200 kHz, with 10 kHz steps.

It is worth pointing out that the input resistance and capacitance of the NI-5922 are 1 MΩ and 60 pF. The VDs responses are dependent to the acquisition system impedance. In the following, the errors have to be intended for the combination of dividers and the NI-5922 card.

1) **Step 1:** The phase skew $\delta\varphi_{\text{NI-5922}}$ between the two channels of the oscilloscope card has been measured according to the scheme shown in Fig. 7(a). The input voltage is generated through one NI-PXIe card 5433 channel, which directly supplies two channels of the oscilloscope card 5922. The measured phase skew is

$$\delta\varphi_{\text{NI-5922}} = \Delta\varphi_{m1} = \delta\varphi_{ch_{\text{A0}}} - \delta\varphi_{ch_{\text{A1}}} \tag{1}$$

where $\delta\varphi_{ch_{\text{A0}}}$ and $\delta\varphi_{ch_{\text{A1}}}$ are the phase errors introduced by the channel 0 and 1 of the NI card 5922, respectively. The behavior of $\delta\varphi_{\text{NI-5922}}$ is given in Appendix B.

In the first step, the intrinsic SF error introduced by the digitizer card (SF_{m0}) is measured. The related equations are as follows:

$$S_0 = \frac{V_{\text{in}}}{V_{00}} \tag{2}$$

$$S_1 = \frac{V_{\text{in}}}{V_{10}}. \tag{3}$$

By combination of (2) and (3)

$$\text{SF}_{m1} = \frac{V_{00}}{V_{10}} = \frac{S_1}{S_0} \tag{4}$$

while S_0 and S_1 are the internal SF*s* introduced by the channels (0 and 1) of the digitizer card, respectively.

2) **Step 2:** The SF and phase error characterization of the CVD1 is measured using the setup scheme shown in Fig. 7(b). The same input of CVD1 is directly connected to channel 1 of the 5922 card (ch_{A1}), while its output is connected to ch_{A0}. In this case, the maximum input amplitude is 5 V, in agreement with the card specifications.

The phase difference measured in this situation between ch_{A0} and ch_{A1} is called $\Delta\varphi_{m2}$. The error introduced by CVD1, $\Delta\varphi_{\text{CVD1}}$ in the following, can be calculated as follows:

$$\Delta\varphi_{\text{CVD1}} = -\delta\varphi_{ch_{\text{A0}}} + \delta\varphi_{ch_{\text{A1}}} + \Delta\varphi_{m2}. \tag{5}$$

With summation of (1) and (5)

$$\Delta\varphi_{\text{CVD1}} = \Delta\varphi_{m2} - \Delta\varphi_{\text{NI-5922}}. \tag{6}$$

The same measurement introduces the SF of CVD1 (SF_1), which can be calculated using the following equation:

$$V_{\text{in}} = \text{SF}_1 \cdot S_0 \cdot V_{01} \tag{7}$$

$$V_{\text{in}} = S_1 \cdot V_{11} \tag{8}$$

$$\text{SF}_{m2} = \frac{V_{01}}{V_{11}} \tag{9}$$

where SF_{m2} is the SF directly measured in this step. By a combination of (4), (7)–(9), SF_1 is obtained as

$$\text{SF}_1 = \frac{\text{SF}_{m1}}{\text{SF}_{m2}}. \tag{10}$$

3) **Step 3:** In the third step, CVD1 and CVD2 are connected to the same input voltage, while their output is connected to ch_{A0} and ch_{A1} of the card 5922, respectively, according to Fig. 7(c). The maximum input voltage is about 50 V, in order to comply with the acquisition card specifications.

The phase difference measured in this situation between ch_{A0} and ch_{A1} is called $\Delta\varphi_{m3}$. Then, the phase error introduced by the CVD2, in the following $\Delta\varphi_{\text{CVD2}}$, can be calculated as

$$\Delta\varphi_{\text{CVD2}} = \delta\varphi_{ch_{\text{A0}}} - \delta\varphi_{ch_{\text{A1}}} + \Delta\varphi_{\text{CVD1}} - \Delta\varphi_{m3}. \tag{11}$$

From (1) and (11)

$$\begin{aligned}\Delta\varphi_{\text{CVD2}} &= \Delta\varphi_{\text{NI-5922}} + \Delta\varphi_{\text{CVD1}} - \Delta\varphi_{m3} \\ &= \Delta\varphi_{\text{NI-5922}} + \Delta\varphi_{m2} - \Delta\varphi_{\text{NI-5922}} - \Delta\varphi_{m3} \\ &= \Delta\varphi_{m2} - \Delta\varphi_{m3}.\end{aligned} \tag{12}$$

The same measurement introduces the SF of CVD2 (SF_2). The latter can be calculated as

$$V_{\text{in}} = \text{SF}_1 \cdot S_0 \cdot V_{02} \tag{13}$$

$$V_{\text{in}} = \text{SF}_2 \cdot S_1 \cdot V_{12} \tag{14}$$

$$\text{SF}_{m3} = \frac{V_{02}}{V_{12}} \tag{15}$$

where SF_{m3} is the measured SF at third step. By combining (4), (10), (11), (13), and (14)

$$\text{SF}_2 = \frac{\text{SF}_{m3}}{\text{SF}_{m2}}. \tag{16}$$

4) **Step 4:** In the final step, CVD2 is used for obtaining the phase error of the RCVD. The RCVD and CVD2 are connected to the same input voltage, while their outputs are connected to ch_{A0} and ch_{A1} of the card 5922, respectively, according to Fig. 7(d). The input voltage amplitude up to 150 V is applied to the dividers. The phase difference measured in this situation between ch_{A0} and ch_{A1} is called $\Delta\varphi_{m4}$. The phase error introduced by the RCVD, $\Delta\varphi_{\text{RCVD}}$ in the following, can be calculated as

$$\begin{aligned}\Delta\varphi_{\text{RCVD}} &= -\Delta\varphi_{\text{NI-5922}} + \Delta\varphi_{\text{CVD2}} + \Delta\varphi_{m4} \\ &= -\Delta\varphi_{m1} + \Delta\varphi_{m2} - \Delta\varphi_{m3} + \Delta\varphi_{m4}.\end{aligned} \tag{17}$$

Fig. 8. Second method measurement setup for SF characterization of the RCVD up to 100 kHz.

The same measurement introduces the SF of RCVD (SF_{RCVD}), which can be calculated as

$$V_{\text{in}} = \text{SF}_{\text{RCVD}} \cdot S_0 \cdot V_{03} \tag{18}$$

$$V_{\text{in}} = \text{SF}_2 \cdot S_1 \cdot V_{13} \tag{19}$$

$$\text{SF}_{m4} = \frac{V_{03}}{V_{13}} \tag{20}$$

where SF_{m4} is the measured SF at the current step. By a combination of (10), (16), (18)–(20), the SF of the RCVD is defined as

$$\text{SF}_{\text{RCVD}} = \frac{\text{SF}_{m1} \cdot \text{SF}_{m3}}{\text{SF}_{m2} \cdot \text{SF}_{m4}}. \tag{21}$$

B. Second Method for the SF Measurement and Results

In addition to the step-up procedure, a second method has been applied to the RCVD to characterize the SF versus frequency. Such an SF characterization is performed in two separate steps; for dc and ac, by the same measurement setup. The input voltage of the RCVD is produced using the Fluke 5700A and its joint amplifier 5725A for voltage up to 200 V and frequency up to 100 kHz.

Both the input and output of the RCVD are measured by two Agilent 3458A multimeters, which have been calibrated before the measurement by a Fluke 5790A ac measurement standard (Fig. 8) at an accuracy better than 100 ppm.

The ratio error, ε_r is defined as

$$\varepsilon_r = \frac{\text{SF}_m - \text{SF}_r}{\text{SF}_r} \tag{22}$$

where SF_m is the measured SF and SF_r is the rated SF equal to 197.90. The result of the ratio error measurements performed by the two methods is shown in Fig. 9. In this figure, the expanded uncertainties at the level 95% probability are shown for both methods. For the first method (step-up) in the evaluation of the uncertainties, the following components have been taken into consideration:

1) The repeatability of the data in every step of the calibration procedure, estimated as the standard deviation.
2) The measured SF variation as a function of the variation in the applied voltage, which was computed repeating the measurements at different voltages, in a given range where the voltage of the output of each CVD is still measurable with a good accuracy. The variation in the SF with the voltage is computed by the difference, at every frequency, between the maximum and minimum values

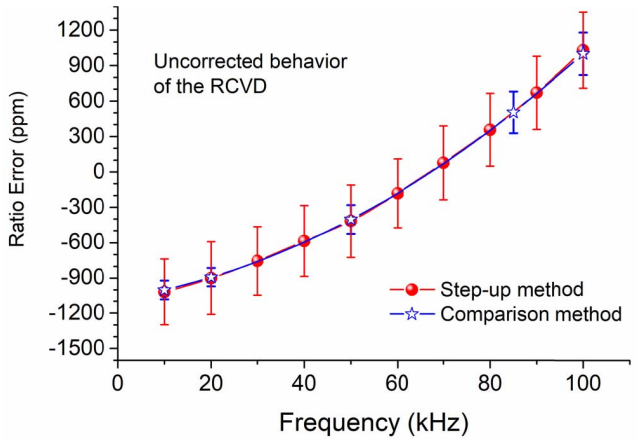

Fig. 9. Ratio error of the RCVD between 10 and 100 kHz.

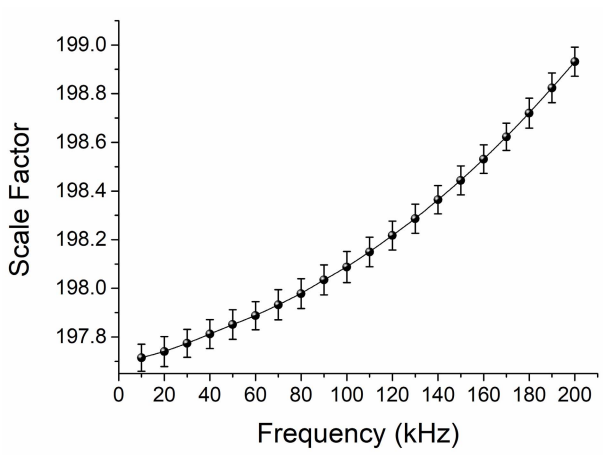

Fig. 10. SF behavior of the RCVD between 10 and 200 kHz.

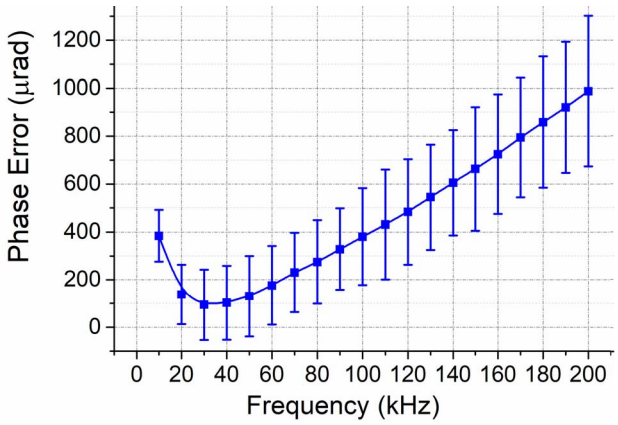

Fig. 11. Phase error behavior of the RCVD versus frequency from 10 to 200 kHz.

measured, divided by the voltage ratio measured by NI card 5922. Such a result is then extrapolated by multiplying it by the ratio between the voltage measured at the next step and the voltage measured at the current step. This component was considered with a rectangular distribution.

3) The crosstalk (110 dB–100 kHz and 100 dB–1 MHz).
4) The resolution (20 bits at 5 MSamples/s used in the acquisition). These two components (resolution and crosstalk) given by the manufacturer specifications, significantly affects only the lower voltages measured in the step-up procedure.
5) The nonlinearity of the digitizer found in technical literature [19]. For every measured voltage, the worst case was considered and the uncertainty components were computed. The rectangular distribution was applied.
6) The medium-term variation of the SF measured by the step-up procedure in a time span of 15 weeks. The calculation of this component (which is not negligible for the SF) can be avoided if the step-up procedure is always performed before using the RCVD. In our uncertainty budget, this term was included.

In the second method, the uncertainty is equal to 180 ppm at 100 kHz. As can be seen, both methods can give very similar results with the differences lower than 30 ppm. However, the proposed step-up method (the first method) could be applied concurrently with the measurement of the phase error, reducing calibration cost and time, besides increasing the frequency bandwidth compared to the currently used calibration methods up to 1 kV.

The SF curve versus frequency, up to 200 kHz, is shown in Fig. 10. The repeatability of the SF measurements shows a variation lower than 100 ppm at 200 kHz in a period of 24 h, which was verified to be stable after some weeks. Long-term stability is currently under investigation.

The characterization has been performed in a voltage range lower than the rated voltage. However, according to [17], the RCVD voltage linearity has been verified from 100 V up to 1 kV. An SF variation lower than 80 ppm has been found, which reduces to 50 ppm upon 1 h warming up time.

C. Measurement of the Phase Error (Results)

The phase error behavior of the RCVD is shown in Fig. 11. As can be seen, the maximum phase error is lower than 1 mrad at 200 kHz, which could be considered a satisfactory result for a reference voltage transducer.

The graph bars in Fig. 11 show the expanded uncertainties (95%) at every frequency. They have been computed using the same method and the same type of components as for the SF uncertainties. Concerning repeatability, Fig. 12 shows the phase error measured at 200 kHz with the divider supplied with the amplitude of 150 V. The measurement is automatically repeated for 48 h every ∼1.5 min. The result shows good repeatability of the *phase error*, which was verified to be stable after many weeks. Long-term stability is currently under investigation.

Fig. 11 also shows a rise in the phase error below 40 kHz. This has been confirmed repeating the step-up procedure in this frequency range by using step-up resistive dividers instead of the step-up CVDs.

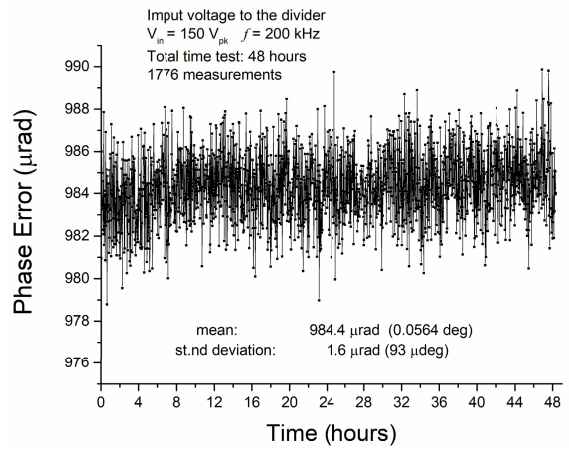

Fig. 12. Repeatability test of the RCVD phase error. This latter is reported versus time, being measured continuously at 200 kHz for 48 h, by automatic measurements.

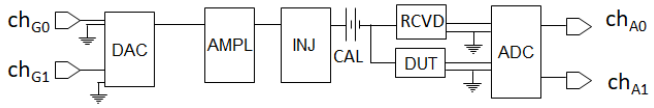

Fig. 13. Schematic of the circuit for the calibration of the commercial probes.

V. Calibration of a Commercial Voltage Transducer

The 1-kV commercial differential voltage probe whose behavior is shown in Fig. 1(b) has been chosen as device under test (DUT) for calibration with the RCVD. This DUT was selected because it is one of the most accurate transducers found in the market.

For the characterization of the probe, the scheme shown in Fig. 7(d) has been applied, substituting CVD2 with DUT and correcting the results according to the calibration results of RCVD. The ac signal is produced by NI 5433 generation card controlled by the LabVIEW program. This ac signal is amplified by the NF amplifier HSA 4052A up to 150 V_{pk}. This voltage is in series with the calibrator FLUKE 5500A through the voltage injector. The circuital scheme is reported in Fig. 13. The dc + ac signal is applied to both the reference RCVD and the DUT, in parallel.

Two probes of the same model have been characterized, called in the following "*probe 1*" and "*probe 2*." Characterization has been carried out with a constant dc voltage equal to 400 V and ac voltage which has been varied from 30 V to 150 V_{pk}. Characterization results are shown in Fig. 14 for what concern the ratio behavior versus frequency, and in Fig. 15 concerning the phase error versus frequency.

The results are consistent with the preliminary ones shown in Section II, with a ratio error of the order of 0.2%, 0.4%. *Probe 1* shows a higher dependence on ac voltage amplitude, whereas *probe 2* is practically independent of this parameter. The same can be observed in the phase error behavior, where the dependence on amplitude of *probe 2* is lower. The phase error shows a pseudolinear behavior above 20 kHz, and is of

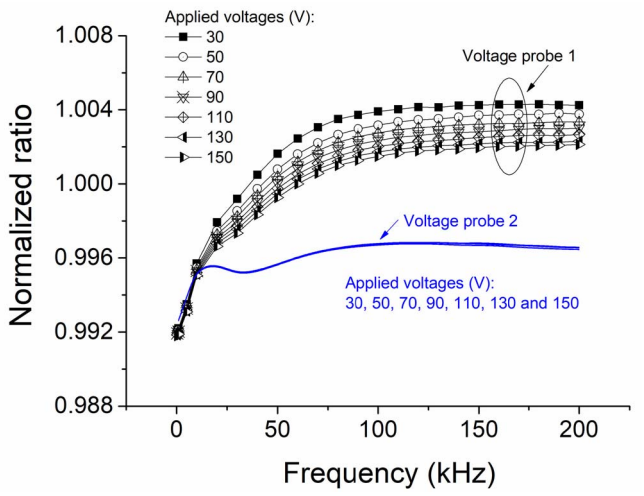

Fig. 14. Normalized ratio behavior of the DUTs versus frequency.

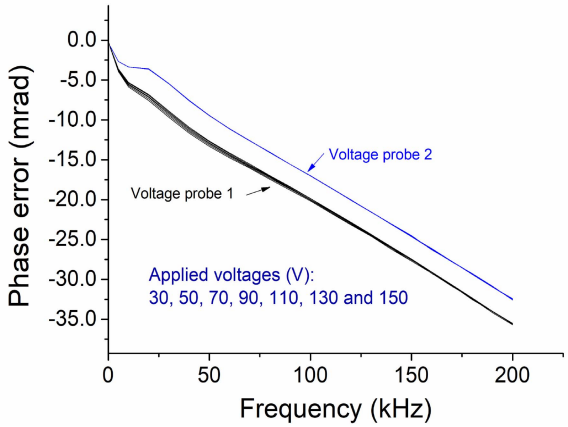

Fig. 15. Phase error behavior of the DUTs versus frequency.

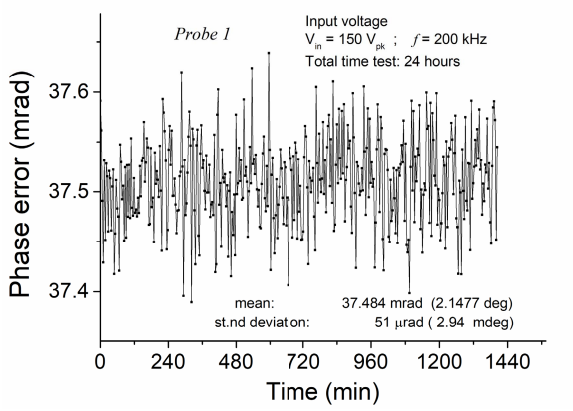

Fig. 16. Phase error repeatability of the *probe 1* DUT tested continuously in 24 h.

the order of ∼17.5 mrad (1°) at 100 kHz (1.15° *probe 1*, 0.97° *probe 2*) and 2° at 200 kHz (2.04° *probe 1*, 1.86° *probe 2*).

Fig. 16 shows the phase error of *probe 1* at 200 kHz continuously measured for 24 h every 3.5 min. The results show a standard deviation of 51 μrad (2.94 mdeg). This result suggests that, upon a proper preliminary calibration of the

probes and compensating their behavior, it is possible to use them for power measurement purposes. The commercial probes show a fairly good stability. Indeed, calibrations repeated in a time span of four months, shows a variation in the SF lower than 0.2% and a variation in the phase angle lower than 0.5 mrad, up to 200 kHz.

VI. Conclusion

Energy conversion and new inductive charging systems for EVs need new and traceable measurement systems for voltage, current, and power. In this framework, this paper presented a reference VD for measuring ac plus dc voltages up to 1000 V, with ac content up to ∼15%. Such values can be found in the above-mentioned applications, and the divider can measure dc voltage plus ac component ripple in the frequency band between 10 and 200 kHz. The realized resistive-capacitive divider shows high stability and good measurement accuracy. The 100 kHz ratio error ε_r is $\leq 10^{-3}$, with a variation lower than 100 ppm, verified over 24 h and repeated a few weeks later. ε_r was determined with a measurement uncertainty of the order of 180 ppm at 100 kHz. At 200 kHz, the ratio error rises to about $5.4 \cdot 10^{-3}$, remaining, however, repeatable. The 100 kHz angle error is ≤ 400 μrad whereas at 200 kHz, it is ≤ 1 mrad, determined with an expanded measurement uncertainty ≤ 300 μrad at 200 kHz. The repeatability of the phase error is good, with absolute maximum variations in the 24 h of 12 μrad and a standard deviation on 1776 measurements of 1.6 μrad.

The high measurement repeatability allows one to correct the ratio and angle errors of the divider, bringing its measurement uncertainty compliant with the design target, which is $0.5 \cdot 10^{-3}$.

This divider is presently unique of its kind in terms of performances and accuracy. Its calibration is currently difficult not only at INRiM but also in many other laboratories; traceability of the SF and of the phase error above 100 kHz is limited to 20 V. This paper presented a calibration method based on a step-up procedure suitable for calibration up to some hundreds of kilohertz and some hundred volts. Overlapping the calibration results to the ones of a well-established method up to 100 kHz, excellent results were found, with a discrepancy on the ratio error lower than 85 ppm.

This paper also presented a voltage measurement chain, based on the reference divider mentioned above and on a voltage injector that allows adding an ac signal with a dc signal maintaining the galvanic separation between the generated ac and the dc generator. Through this voltage chain, it is possible to calibrate the commercial voltage meters that can be used in IPT applications.

This paper presented the results of the calibration of one of the best commercial transducers available on the market, both in terms of ratio and phase errors. The possibility to calibrate these dividers and to correct the response, especially in phase, is very interesting to realize power measurements that do not expose expensive power analyzers to the transients that can be found in the charging stations.

Finally, this paper illustrated how the voltage chain can be used, in perspective, in the realization of ac power standard based on phantom power. The detailed discussion of this topic, as well as the long-term stability of the system, go beyond the purpose of this paper and will be the object of the continuation of this study.

Appendix

A. Circuit Tuning

Making reference to Fig. 3(a), it is important to set the relationship between voltage and current measurement chains. To do this, it is possible to take the generation and acquisition of the other chain as a reference, the latter considered in direct connection between the generation and acquisition channels. In the case of tuning, the voltage channel [see Fig. 2(b)] zero is the reference.

An automatic program developed in LabVIEW is able to store the measured phase difference between acquisition channel 0 and 1, for different values of the generated voltage amplitude (ampl) and frequency (f)

$$\boldsymbol{\varphi}_{\mathrm{VTUN}} = \varphi_{\mathrm{VTUN}}(\mathrm{ampl}, f) \tag{A1}$$

being

$$\varphi_{\mathrm{VTUN}} = \varphi_{ch\upsilon_{\mathrm{A0}}} - \varphi_{ch\upsilon_{\mathrm{A1}}} = \Delta\varphi_{(ch\upsilon_{\mathrm{A0}}-ch\upsilon_{\mathrm{A1}})} \tag{A2}$$

where $\Delta\varphi_{(ch\upsilon_{\mathrm{A0}}-ch\upsilon_{\mathrm{A1}})}$ is the uncorrected phase difference between the two channels.

Moreover

$$\varphi_{ch_{\mathrm{A0}}} = \delta\varphi_{ch_{\mathrm{G0}}} + \delta\varphi_{ch_{\mathrm{A0}}} \tag{A3}$$

$$\varphi_{ch_{\mathrm{A1}}} = \delta\varphi_{ch_{\mathrm{G1}}} + \Delta\varphi_{\mathrm{VSC}} + \Delta\varphi_{\mathrm{RCVD}} + \delta\varphi_{ch_{\mathrm{A1}}} \tag{A4}$$

$$\varphi_{\mathrm{VTUN}} = (\delta\varphi_{ch_{\mathrm{G0}}} - \delta\varphi_{ch_{\mathrm{G1}}}) + (\delta\varphi_{ch_{\mathrm{A0}}} - \delta\varphi_{ch_{\mathrm{A1}}}) - \Delta\varphi_{\mathrm{VSC}} - \Delta\varphi_{\mathrm{RCVD}} \tag{A5}$$

where $\delta\varphi_{ch_{\mathrm{A0}}}$ and $\delta\varphi_{ch_{\mathrm{A1}}}$ are the phase errors introduced by the channels 0 and 1 of the NI card 5922, respectively, and $\delta\varphi_{ch_{\mathrm{G0}}}$ and $\delta\varphi_{ch_{\mathrm{G1}}}$ are the phase errors introduced by the channels 0 and 1 of the NI card 5433, respectively.

Similarly, for the current chain, the phase angle can be written as

$$\varphi_{\mathrm{ITUN}} = \varphi_{chI_{\mathrm{A0}}} - \varphi_{chI_{\mathrm{A1}}} = \Delta\varphi_{(chI_{\mathrm{A0}}-chI_{\mathrm{A1}})} = (\delta\varphi_{ch_{\mathrm{G0}}} - \delta\varphi_{ch_{\mathrm{G1}}}) + (\delta\varphi_{ch_{\mathrm{A0}}} - \delta\varphi_{ch_{\mathrm{A1}}}) + \Delta\varphi_{\mathrm{CSC}} + \Delta\varphi_{\mathrm{RSH}} \tag{A6}$$

where $(\delta\varphi_{ch_{\mathrm{G0}}} - \delta\varphi_{ch_{\mathrm{G1}}})$ represents the skew between generation channels. For the considered digital-to-analog converter (DAC), the value depends on amplitude and frequency and its value varies from ∼15 μrad at 1 kHz to ∼−350 μrad at 200 kHz with 150 V input amplitude. $(\delta\varphi_{ch_{\mathrm{A0}}} - \delta\varphi_{ch_{\mathrm{A1}}})$ represents the skew between the acquisition channels. It is independent of the input amplitude and it has a linear behavior versus frequency, which is stable versus time. Its value varies from −1.75 μrad at 1 kHz to −265 μrad at 200 kHz. Concerning the measurement of the skew between channels, see Appendix B.

$\Delta\varphi_{\mathrm{VSC}}$ is the main angle term, so that $\Delta\varphi_{\mathrm{VSC}} \approx \varphi_{\mathrm{VTUN}}$, which is mainly due to the voltage amplifier (∼24°/420 mrad at 200 kHz). Its behavior, versus frequency is shown in Fig. 17 and is dependent on the ac voltage amplitude but

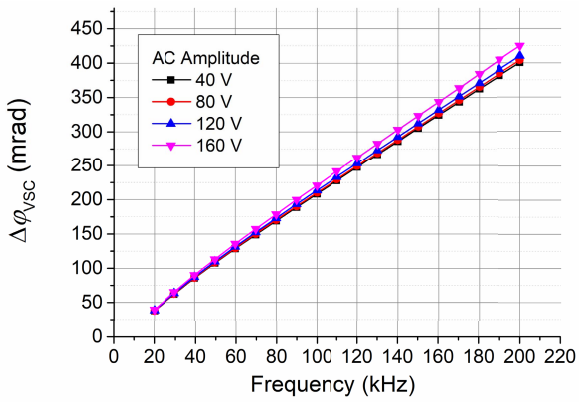

Fig. 17. Measured phase shift of the voltage chain, mainly due to the ac voltage amplifier. The curves are independent of the applied dc voltage bias. Tested with ac voltage amplitudes specified in the picture plus dc voltages equal to 50, 200, and 500 V (curves overlapped).

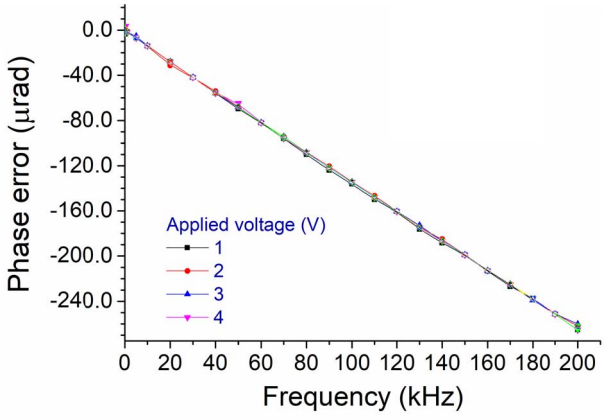

Fig. 18. Phase skew between acquisition channels of the 5922 card.

not of the dc voltage component. $\Delta\varphi_{\mathrm{RCVD}}$ is the phase error of the RCVD measured during its calibration, which is lower than 1 mrad at 200 kHz (see Section IV-C).

The phase φ_V in input to the RCVD [see Fig. 3(a)] is obtained as

$$\varphi_V = \varphi_{\mathrm{VTUN}} - \Delta\varphi_{\mathrm{RCVD}} - (\delta\varphi_{ch_{\mathrm{A0}}} - \delta\varphi_{ch_{\mathrm{A1}}}). \quad \text{(A7)}$$

Similarly, for the current, the phase angle can be written as

$$\varphi_I = \varphi_{\mathrm{ITUN}} - \Delta\varphi_{\mathrm{RHS}} - (\delta\varphi_{ch_{\mathrm{A0}}} - \delta\varphi_{ch_{\mathrm{A1}}}) \quad \text{(A8)}$$

where φ_{VTUN}, φ_{ITUN}, and $(\delta\varphi_{ch_{\mathrm{A0}}} - \delta\varphi_{ch_{\mathrm{A1}}})$ are measured, while $\Delta\varphi_{\mathrm{RCVD}}$ and $\Delta\varphi_{\mathrm{RSH}}$ come from calibration (see Section IV for the RCVD calibration).

It is worth to note that the difference $\varphi_V - \varphi_I$ is independent of the acquisition channel skew, being

$$\varphi_V - \varphi_I = \varphi_{\mathrm{VTUN}} - \Delta\varphi_{\mathrm{RCVD}} - \varphi_{\mathrm{ITUN}} + \Delta\varphi_{\mathrm{RHS}}. \quad \text{(A9)}$$

To set the phase of the phantom power to the desired value α it is needed to supply the voltage chain with a phase $(-\varphi_V + \alpha)$ and the current chain with a phase $(-\varphi_I)$.

Concerning the voltage chain, which is the subject of this paper, the authors used an automatic calibration program able to perform a preliminary alignment of the chain, and to apply the compensation $(-\varphi_V + \alpha)$ for the phase and the one for amplitude. The latter requires a preliminary calibration by applying different amplitudes at different frequencies to ch_{G1} and calculating the transfer matrix as

$$\mathbf{TM} = \frac{V_{ch_{\mathrm{G1}}}(\mathrm{ampl}, f)}{V_{ch_{\mathrm{A1}}}(\mathrm{ampl}, f)}. \quad \text{(A10)}$$

Through the SF of the RCVD, as determined in Section IV-B, which is independent of the amplitude, the voltage applied to the divider is

$$V_{\mathrm{appl}}(\mathrm{ampl}, f) = \mathrm{SF}(f) \cdot V_{ch_{\mathrm{A1}}}(\mathrm{ampl}, f). \quad \text{(A11)}$$

To obtain the desired applied voltage, the following computation is done:

$$V_{ch_{\mathrm{G1}}}(\mathrm{ampl}, f) = \mathbf{TM} \cdot \frac{V_{\mathrm{appl}}(\mathrm{ampl}, f)}{\mathrm{SF}(f)}. \quad \text{(A12)}$$

The desired voltage amplitude at the divider is obtained within the divider accuracy, which is described in Section IV-B.

The phase tuning is more complex since the phase also depends on the behavior of ch_{G0}, which is the reference for the voltage phase measurement. The results obtained are different depending on whether a multilayered approach or a simple matrix is applied. The simple matrix is obtained by applying the same amplitude to both generation channels. However, the response of the chosen generation card, unlike the acquisition card, varies when the amplitude of the signal generated by the two channels is different. In the multilayer approach by varying the amplitudes of the ch_{G1} channel, a calibration matrix is obtained for each single amplitude applied to the ch_{G0} channel. In the multilayer approach, the alpha angle can be settled with an accuracy close to 0.02° (350 μrad), in the second case, the value in the worst situation becomes 10 times larger (0.2° or 3.5 mrad).

B. Acquisition Card Characterization

By imposing the same input to the two acquisition channels, as shown in Fig. 7(d), with different amplitudes, the ratio error between the two channels has been measured resulting to be slightly dependent on the amplitude and, in any case, lower than 35 ppm. The phase delay between the two channels results to be linear and independent of the amplitude (Fig. 18).

For the PXI 5922 card used, at 200 kHz, the delay is 264 μrad, which corresponds to a temporal skew of 210 ps. We found this value repeatable, as shown in Fig. 19. The result obtained is consistent with the skew between the acquisition channels stated by the manufacturer, which is $\leq$500 ps up to 1 MHz.

C. Characterization of the Voltage Injector

The characterization of the voltage injector requires the preliminary calibration of the RCVD reference divider. This latter is done according to the four steps described in Section IV. An additional step is obtained using the scheme shown in Fig. 20. A voltage level between 20 and 160 V is applied as input to the reference divider and to the injector by a voltage amplifier, with frequencies between

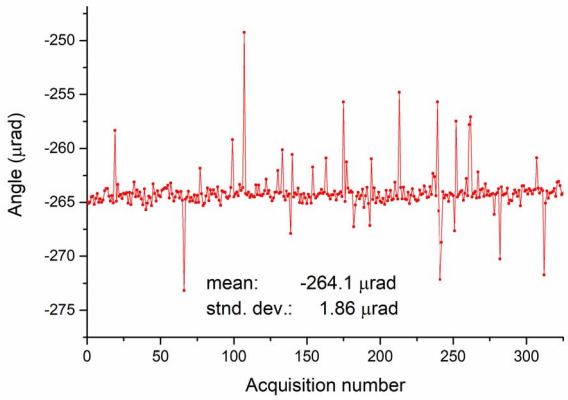

Fig. 19. Phase error repeatability of the *probe 1*, DUT tested continuously in 24 h at 200 kHz.

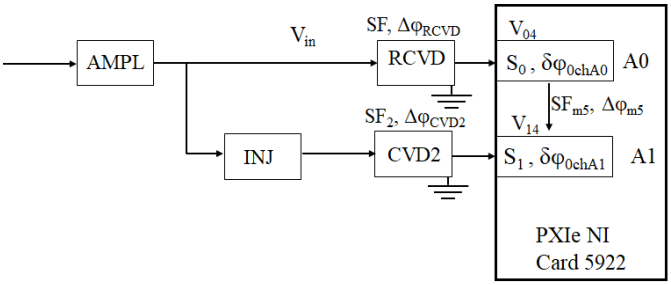

Fig. 20. Setup for the characterization of the voltage injector (INJ in the scheme).

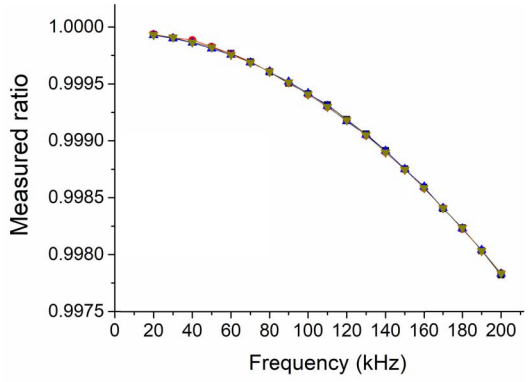

Fig. 21. Measured ratio of the voltage injector.

20 and 200 kHz. Since the injector ratio is about 1, it is necessary to use CVD2 to reduce the ADC input voltage at a level $\leq$5 V.

Making reference to Section IV, in this additional step (Step 5), the following SF is measured according to Fig. 20:

$$\mathrm{SF}_{m5} = \frac{V_{04}}{V_{14}} \tag{C.1}$$

$$V_{\mathrm{in}} = \mathrm{SF}_{\mathrm{RCVD}} \cdot S_0 \cdot V_{04} \tag{C.2}$$

$$V_{\mathrm{in}} = \mathrm{SF}_{\mathrm{inj}} \cdot \mathrm{SF}_{\mathrm{CVD2}} \cdot S_0 \cdot V_{04} \tag{C.3}$$

$$\mathrm{SF}_{\mathrm{inj}} = \frac{\mathrm{SF}_{m5}}{\mathrm{SF}_{m4}}. \tag{C.4}$$

Concerning the phase shift, this is computed as

$$\Delta\varphi_{\mathrm{INJ}} = \Delta\varphi_{\mathrm{NI\text{-}5922}} - \Delta\varphi_{\mathrm{CVD2}} - \Delta\varphi_{m5} + \Delta\varphi_{\mathrm{RCVD}} \tag{C.5}$$

$$\Delta\varphi_{\mathrm{INJ}} = \Delta\varphi_{m4} - \Delta\varphi_{m5}. \tag{C.6}$$

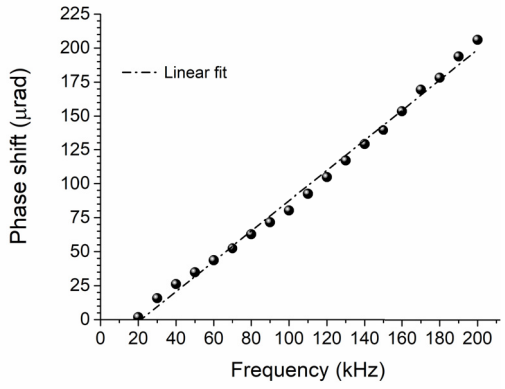

Fig. 22. Measured phase shift (dots) introduced by the voltage injector.

The results of the injector characterization are shown in Figs. 21 and 22, regarding the injector ratio and the phase shift (error), respectively. The injector response is practically independent of the voltage amplitude. The 20 kHz ratio is 0.99993 and reduces to 0.99782 at 200 kHz following a parabolic law. The phase shift introduced by the injector varies almost linearly from 1.7 μrad at 20 kHz up to 210 μrad at 200 kHz.

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