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T.R. 2/2020 January 2020

I.N.RI.M. TECHNICAL REPORT

Abstract

The present Technical Report describes the development of prototype FPGA-based frequency stabilization electronics for compact laser frequency control with the Pound-Drever-Hall technique.
The electronic control system comprised an Altera Cyclone II FPGA board and a daughter board with two 100ks/s 16 bit DA, 50 Ms/s AD and 12 bits DA; it provided a 500 kHz modulation signal obtained with direct digital synthesis and direct demodulation of the sampled frequency error signal.
The automatic lock-relock feature was validated experimentally.

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Pound-Drever-Hall electronics and automatic relock

The automatic relocking of the laser to the same cavity mode is essential for unattended, reliable use in an industrial environment or in space of a compact, robust and turn-key frequency standard.

In this work package we have adopted a solution based on a field programmable gate array (FPGA). The error signal is generated by means of the Pound-Drever-Hall (PDH) method, using digital signal processing (DSP) in the FPGA. The FPGA also allows the whole system to be controlled (changing the locking parameters is very easy) and integrates an automatic, fast relock algorithm to the same cavity mode.

Because all the signals are available in a digitized form and fast DSP is available in the FPGA, other functions can be implemented, *e.g.* to characterize and optimize the laser locking system.

In the FPGA board, the PI filter and the automatic lock/relock feature have been tested in a real system available at INRIM. Typical relock time was found to be less then 20 ms for a cavity with a nominal linewidth of 70 kHz.

System architecture and operation

The system consists of a digitally implemented Pound-Drever-Hall (PDH) modulator-demodulator-lock subsystem, a relock subsystem and a system controller. The PDH signals are converted to/from the analog form by an external I/O board which hosts some A/D and D/A converters.

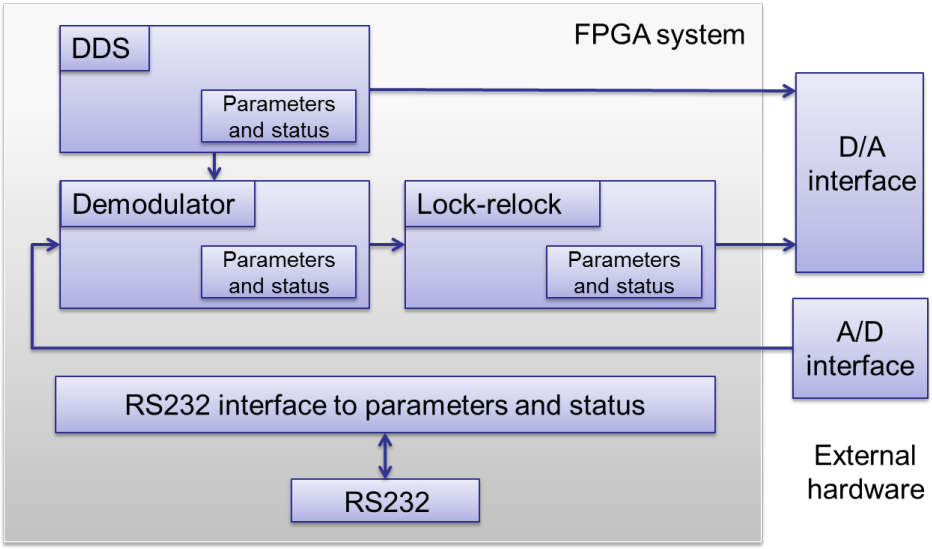

Fig. 1 - System architecture

The laser frequency is first scanned in order to identify the resonance position, then the loop is closed and the lock/relock section behaves like a PI filter.

The parameters of each subsystem can be accessed through a GUI written in JAVA.

EOM_AMPLITUDE	EOMA	R/W	-32768 / 32767	Modulation amplitude
EOM_FREQUENCY	EOMF	R/W	0 / 65535	Modulation frequency
DEMODULATOR_PHASE	DPH	R/W	0 / 65535	Demodulator phase
PID_I	KI	R/W	0 / 255	PID: integrator time constant
PID_P	KP	R/W	0 / 255	PID: proportional coefficient
PID_I2	KI2	R/W	0 / 255	PID: integrator 2 time constant

Fig. 2 - Some of the subsystem parameters accessible with the GUI

The device prototype

The device prototype consists of an Altera Cyclone II evaluation board (on the left) and a custom daughter board (on the right) which hosts the A/D and D/A converters. The device is connected to a PC through an RS232 interface, which allows the FPGA system parameters and status to be accessed as read/write registers.

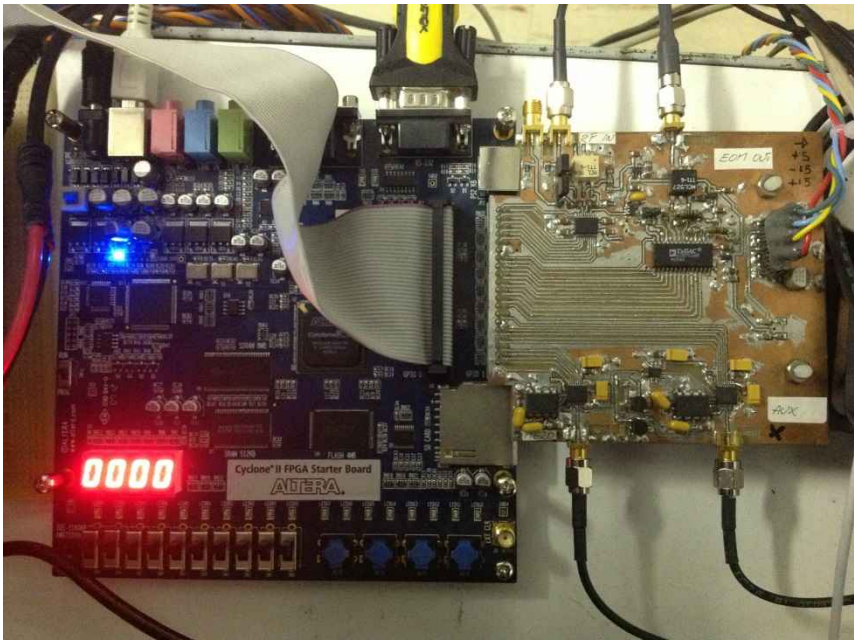

Fig. 3 - The device prototype

A graphical user interface (GUI) has been developed in Java language to easily access the registers.

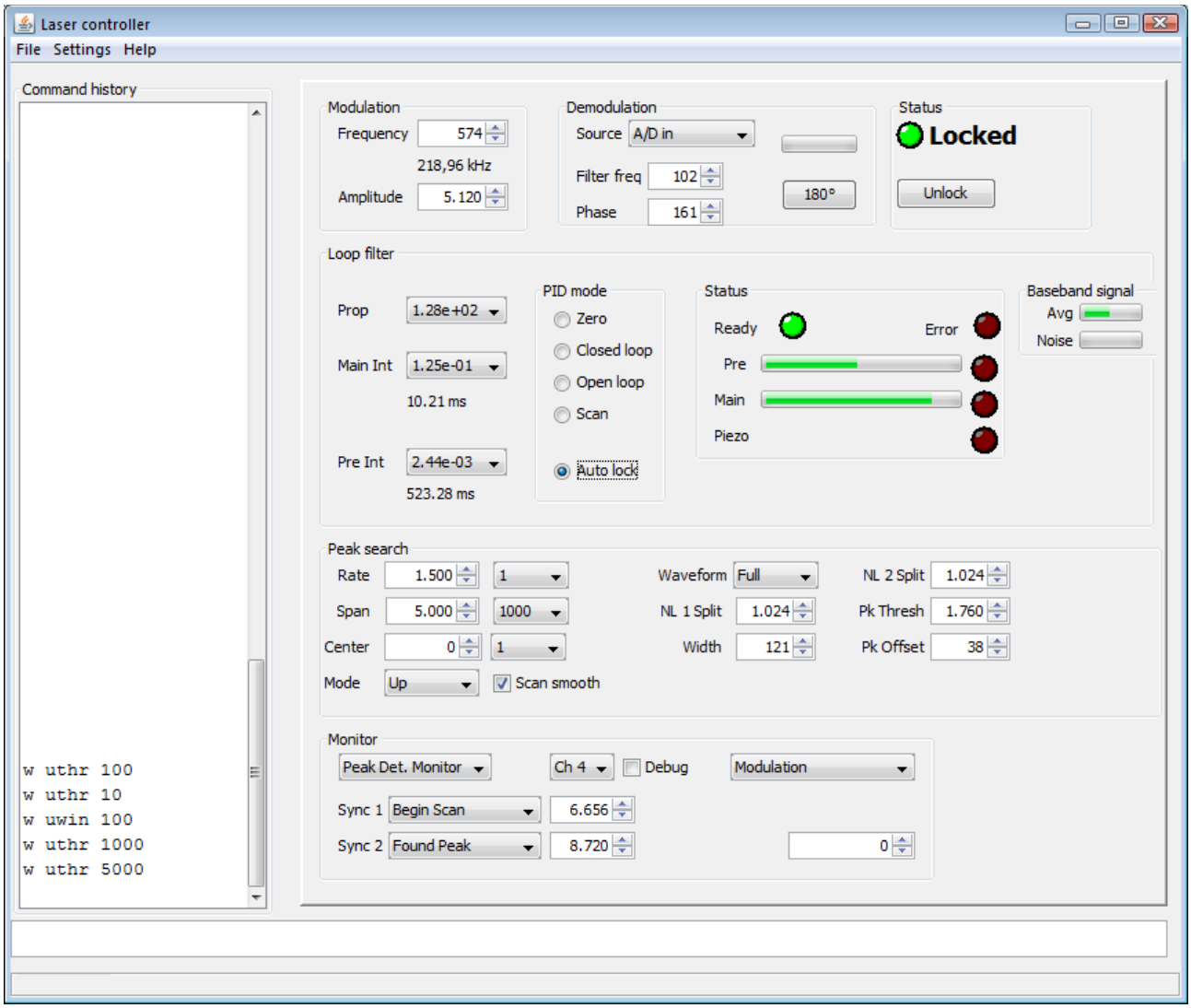

Fig. 4 - GUI interface to the FPGA parameters

Modulator-demodulator subsystem

The subsystem consists of a direct digital synthesizer (DDS) which generates the PDH (phase) modulation frequency which in our case was sent, after D/A conversion, to an electro-optic modulator (EOM) operating at 500 kHz. The DDS frequency can be changed in the range from DC to 25 MHz with a step size of 381 Hz.

A smoothing function has been added as well in order to avoid sudden transients to the EOM device.

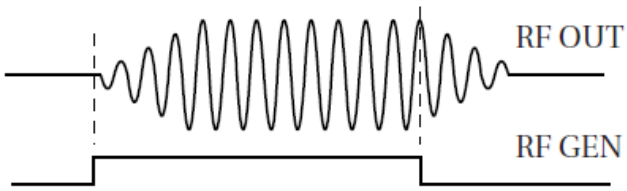

Fig. 5 – Local oscillator smoothing function

According to theory, the returning signal from the photodiode is phase shifted with respect to the modulating signal generated by the local oscillator as depicted in figure 6 where LO is the modulating signal and RF is the returned signal . As the laser-cavity detuning information A(t) has to be extracted, usually a phase shifter is inserted in the radiofrequency signal path. In the digital implementation of the demodulator, the phase is instead shifted after the demodulation has been performed.

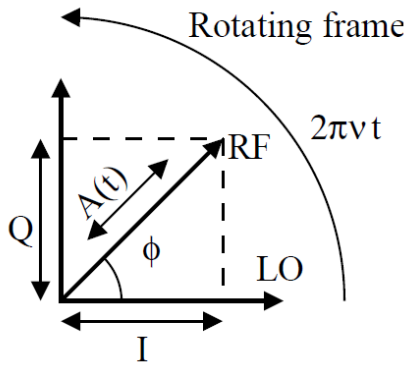

Fig. 6 – Radiofrequency signals

Thus an I-Q demodulator has been designed and the phase has been corrected in the baseband signal path by multiplying the I-Q signals by the frame rotation matrix R

$$[\mathbf{R}] = \begin{bmatrix} \cos\Phi & -\sin\Phi \\ \sin\Phi & \cos\Phi \end{bmatrix}$$

The resulting signal is finally sent to the PI controller.

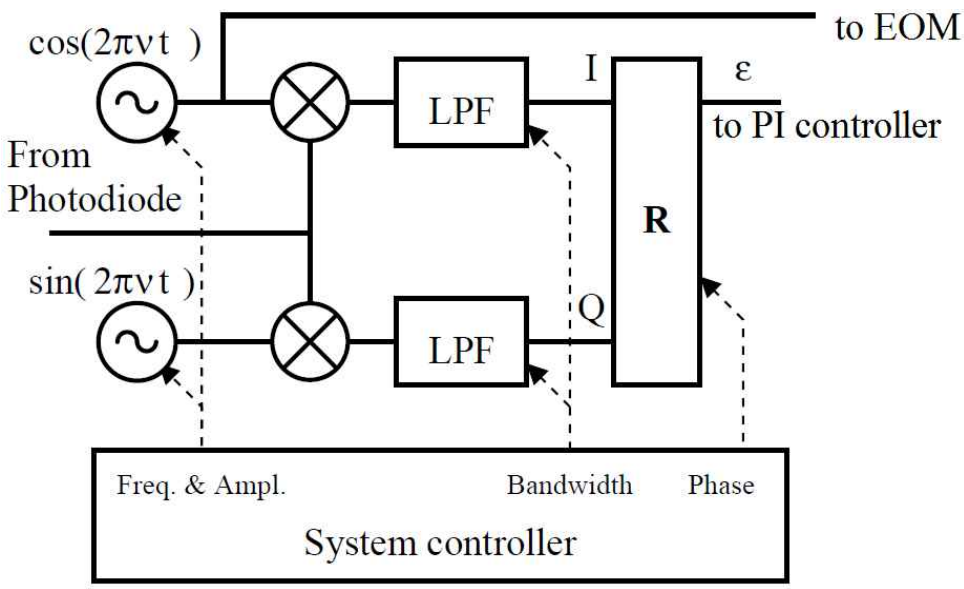

Fig. 7 – Modulator-demodulator subsystem

Lock-relock subsystem

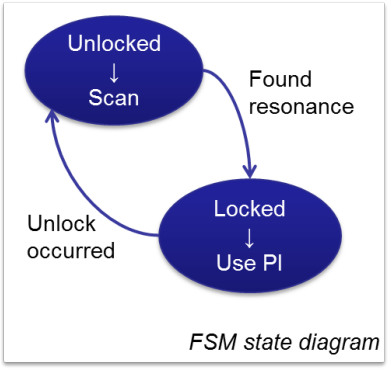

Fig. 8 - Lock/unlock finite state machine diagram

The locked/unlocked condition is kept in a two-state finite state machine (FSM). When the system is in the state «Unlocked», the laser frequency is scanned until a resonance is found. When a resonance is detected, the FSM changes its state to «Locked» and the frequency is stabilized by the PI controller.

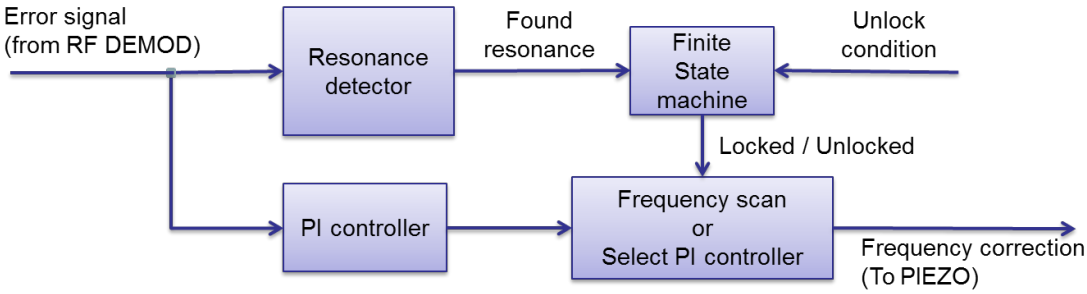

Fig. 9 - Block diagram of the lock-relock subsystem

A frequency scan is performed and the error signal e(t) is processed by a nonlinear function. The signal and a finite length pulse are correlated and then processed by a second, nonlinear function. The maximum of the resulting function a(t) corresponds to the resonance condition.

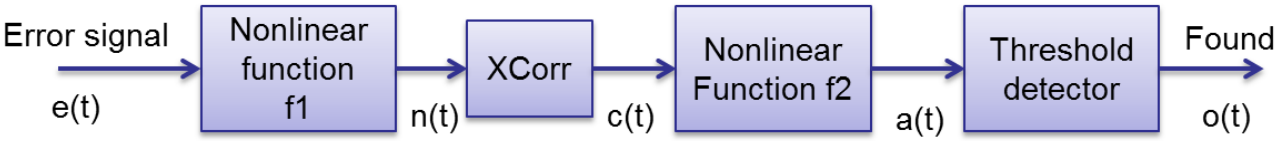

Fig. 10 - Block scheme of the resonance detector

Icarus-Verilog simulation of the resonance detector algorithm

The resonance detector algorithm is implemented in Verilog language in the FPGA, and it operates on the baseband PDH signal.

The algorithm has been validated with an off-line simulator (Icarus Verilog) which generates the ideal PDH signal, e(t), that one would expect to obtain during a scan of the laser frequency in the surroundings of the resonance (the blue curve in the figure).

The PDH signal was calculated and stored, with the corresponding frequency detuning, in a file which was read during the simulation.

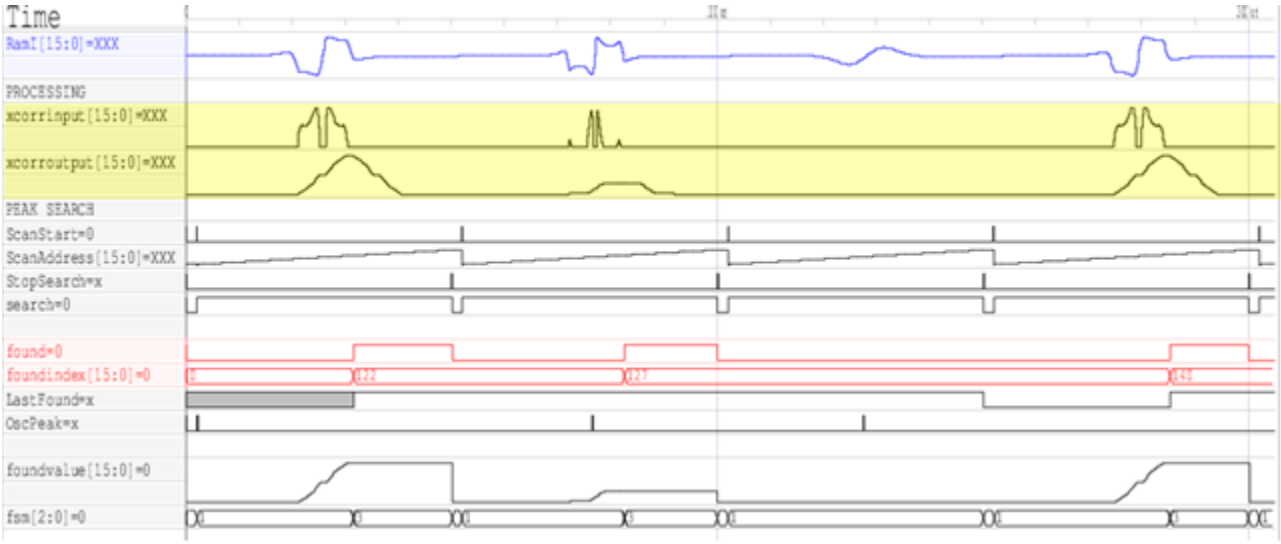

Fig. 11 - Time domain simulation of the unlock detector

For debug purposes, the input n(t) and the output c(t) of the correlator are also shown (yellow highlight in figure).

The *resonance found condition* is shown in red. For every resonance condition, the value of the frequency is stored as a 16 bit number (shown in red); that value will then be used as a starting point around which the PI loop will be closed. The frequency value is corrected in order to compensate for the delay in the signal processing due to the autocorrelation operator.

Validation of the device connected to a laser-cavity system simulator

After the validation of the detector algorithm, a time-domain simulator of the expected signal from the photodiode of a laser-cavity system has been realized inside the FPGA. It consists of an ideal system to which frequency noise has been added.

The simulator consists of an I-Q pair of PDH signals, as expected from an ideal electro-optic setup, stored in a table inside the FPGA. The index of the table represents the laser-cavity detuning Δ which is fed to the simulated laser.

The laser-cavity simulator thus provides the time domain RF signal

$$V_{RF}(t,\Delta,\eta)=I(\Delta+\eta)\cos(\omega t)+Q(\Delta+\eta)\sin(\omega t)$$

where η is the laser frequency, which is simulated inside the FPGA by means of a slightly modified Gold sequence generator.

The simulator code has been inserted at the end of modulator and controller signal paths and the resulting RF signal from the simulated electro-optic setup is sent to the external RF D/A converter.

The D/A feeds the A/D, thus closing the loop on the FPGA.

With this approach it is possible to debug the lock system in ideal conditions directly on the FPGA device. After the debug phase, the simulator code is removed from the firmware while keeping the stabilization code.

An auxiliary D/A converter is used to show on an oscilloscope some internal and monitor signals, together with the digital signals which are available on dedicated pins of the FPGA board (*e.g. resonance found* condition, ...).

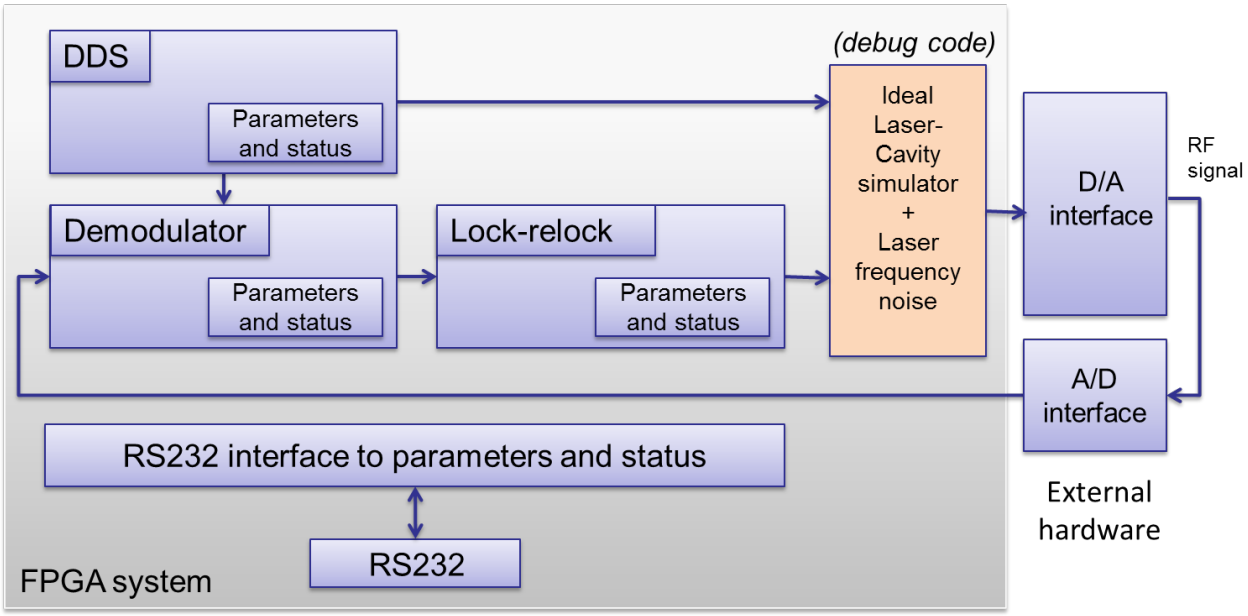

Fig. 12 - Validation of the device with a simulator

Simulation of the resonance identification by scanning a simulated PDH signal with frequency noise

The resonance identification algorithm has been tested with the time-domain simulator. The two D/As were fed with the simulator output, generating the PDH signal in yellow, and with the output a(t) of the second non-linear function of the detector, in light blue. The outputs of the D/As were sent to an oscilloscope in order to be visualized.

The time delay of a(t) with respect to the resonance is caused by the delay in the signal processing and is compensated in the algorithm.

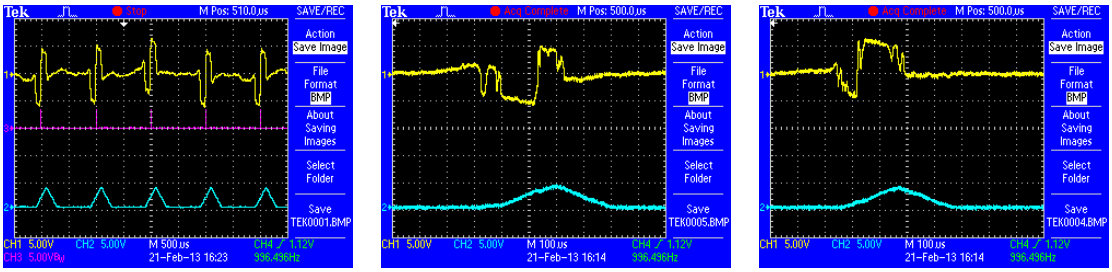

Fig. 13 - Resonance identification with time-domain simulator

Experimental verification of the resonance identification algorithm with real PDH signals

The digital system has been connected to a real electro-optic setup, constituted by a Nd:YAG laser operating at its fundamental and a 70 kHz linewidth cavity. Phase modulation of the laser beam was performed at 500 kHz with an EOM.

A frequency scan has been performed in order to verify the correct operation of the demodulator and of the resonance detector algorithm.

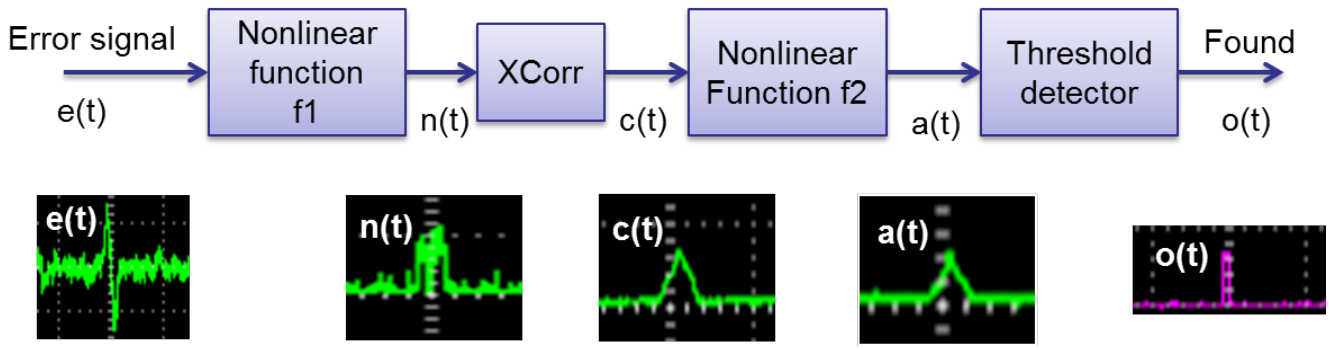

Fig. 14 - Block scheme of the resonance identification algorithm and FPGA internal signals in the real system

The two D/As were fed with the voltage ramp used for the frequency scanning (yellow trace) and with the demodulated signal (green trace). The *resonance found* condition was monitored on a pin of the FPGA board header.

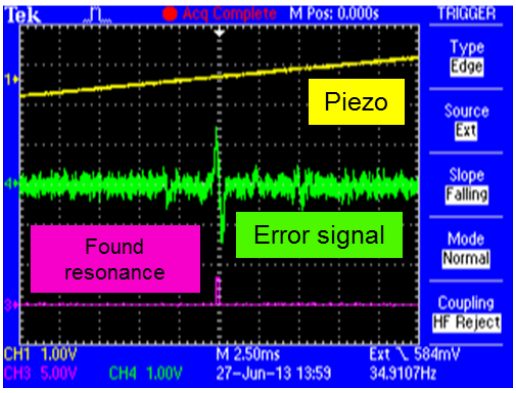

Fig. 15 - Resonance identification as seen on the oscilloscope

Experimental verification of the lock-relock capabilities with a real laser-cavity setup

The lock-relock system has been experimentally validated with the Nd:YAG/cavity setup.

We found a typical relock time below 20 ms. The relock time depends on the linewidth of the resonator (which limits the scan speed) and on the difference between the laser - resonator frequencies when the unlock condition occurs.

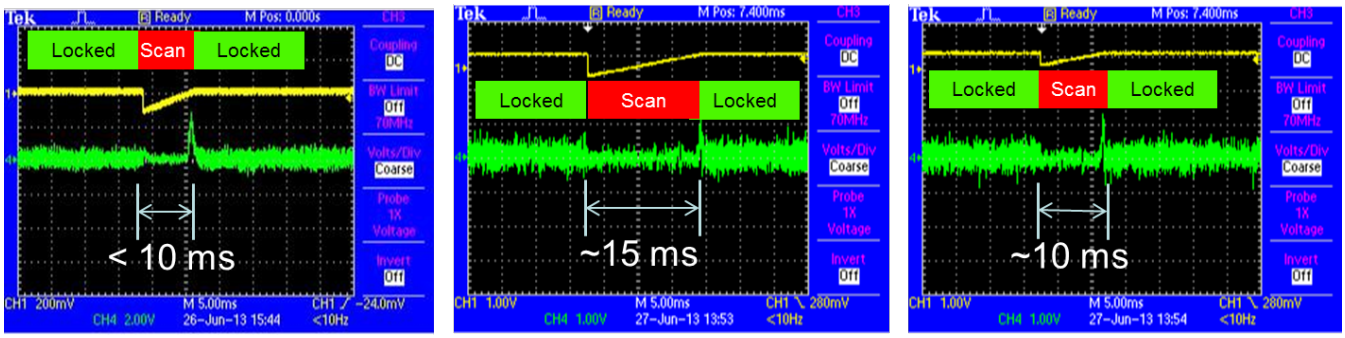

Fig. 16 – Lock/relock with a real system

List of acronyms

A/D	analog to digital converter
D/A	digital to analog converter
DDS	direct digital synthesizer
DSP	digital signal processing
EOM	electro-optic modulator
FPGA	field programmable gate array
FSM	finite state machine
GUI	graphical user interface
PC	personal computer
PDH	Pound-Drever-Hall
PI	proportional-integral