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Metrological Assessment and Simulation of Charge Injection Phenomena in CMOS Electronic Switches

Bruno Trinchera, Paolo Durandetto, and Ricardo Iuzzolino

***Abstract*—This article presents the research activity and key findings from a technical task conducted as part of the True8DIGIT project, funded by the European Partnership on Metrology (EPM) research program. A key objective of this activity was to develop a traceable metrological method for precisely characterizing the charge injection phenomenon in commercial complementary metal–oxide–semiconductor (CMOS) switches, enabling the identification of top-performing devices with minimized charge-induced errors. These switches are critical components in the track-and-hold (T/H) circuits of high-precision integrating digitizers, where charge injection introduces nonlinear distortions that ultimately degrade the digitizer's accuracy. The proposed measurement method enables precise characterization of charge injection in discrete CMOS switches mounted in dedicated chip carriers, utilizing air–dielectric capacitor standards and a traceable digital sampling multimeter. Moreover, the temperature dependence of charge injection was investigated by modifying one of the carrier boards. The experimental setup achieves a resolution of 1 pC, and the Type-A uncertainty ranges from 10 fC to 70 fC, across different CMOS switches. The overall measurement uncertainties did not exceed 7% for charge injection values below 5 pC and 3% for values between 50 and 350 pC. The lowest relative uncertainty achieved was below 0.5% for charge injection in the range 10–40 pC, indicating that charge injection behavior in CMOS switches is strongly dependent on the specific device under test.**

***Index Terms*—Charge-injection devices, complementary metal–oxide–semiconductor (CMOS) switches, measurement techniques, measurement uncertainty, signal sampling.**

I. Introduction

Complementary metal–oxide–semiconductor (CMOS) switches are key components widely used in building the input stage of high-precision digital multimeters [1]—in circuits such as track-and-hold (T/H) and switched-capacitor integrators [2], [3]. They are also applied in multiplexer-based instruments [4], enabling the integration of programmable Josephson voltage standards (PJVS) into practical measurements of ac voltage, current, and electrical power [5]. In particular, CMOS technology combines the benefits of both analog and digital circuits with unprecedented advantages in signal processing and analog-to-digital conversion. Modern CPUs, GPUs, FPGAs, and ASICs have benefited significantly from CMOS technology due to its key advantages. These include reduced transistor dimensions (which enable high device density), ease of fabrication, high noise immunity, higher operating frequencies, low power consumption and leakage, as well as reduced complexity when designing complex systems-on-chip.

A significant drawback of analog CMOS switches used in sampled measurements is their inherent switching-related errors, which compromise the performance of high-precision sampling circuits. Two distinct physical mechanisms are responsible for these errors [1], [3].

1) Clock feedthrough arises from the coupling of the fast on–off clock transitions applied to the control gate to its gate-to-diffusion overlap capacitances. This effect can be treated deterministically as capacitive charge redistribution and leads to a voltage error that is independent of the input voltage, manifesting itself as a constant offset in the input/output characteristic.
2) Channel charge injection occurs because the conducting channel of a CMOS switch stores mobile carriers while the device is on; when the switch turns off, these carriers are released into the source and drain terminals. As emphasized in [3], channel charge injection contributes to CMOS sampling circuits in terms of gain, offset, and nonlinearity errors. Although the first two contributions can be compensated using appropriate measurement calibration strategies, the last can be mitigated using charge injection compensation techniques.

In summary, both effects inject charge into the T/H capacitor, producing a voltage error that degrades measurement accuracy. Separating the two contributions is difficult; what is relevant for this work is an accurate quantification of the overall charge-injection effect under realistic conditions, using sampling frequencies in the kilohertz range. While overlap capacitance (clock feedthrough) can be modeled in a relatively straightforward manner, channel charge injection is considerably more complex, as it depends on multiple parameters such as the intrinsic dimensions of the transistor channel, the instantaneous impedances seen at its terminals with respect to ground, temperature, clock transition time, and other circuit parameters. In fact, lumped equivalent circuits and models are reported in the literature to analyze and

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explore the voltage error dependence in switched capacitors [6], [7], [8], [9], [10]. In many cases, circuit parameters are poorly controlled, and most circuit simulation programs model charge injection in CMOS switches using simplified approaches, which are insufficient to meet the requirements of high-precision measurements.

To bridge this gap, one of the key tasks of the True8DIGIT project [11] is to identify state-of-the-art passive analog components, particularly CMOS analog switches, resistors, and capacitors, suitable for integration into novel amplifiers, such as composite operational amplifiers (COPAs), for use in integrator and front-end digitizer circuitry with zero drift, extremely high gain, low noise, and sub-ppm error. Meeting this error requirement is a critical design specification for realizing an 8.5-digit resolution digitizer. For integrating analog-to-digital converter (IADC), the acceptable level of charge injection must lie in the sub-pC range, as higher levels would compromise accuracy and exceed the project's stringent error limits. Although best-in-class switches are typically specified with charge injection on the order of a few pC, our measurements presented in this article indicate that the tested devices could satisfy the effective requirement when supported by appropriate charge injection compensation techniques, or if novel switches with sub-pC are identified. Furthermore, the project aims to develop advanced numerical simulation models and precise metrological methods for the accurate characterization of these analog components.

This article is an extension of the proceeding paper [12], introducing significant novelties, including: 1) new experimental results on charge injection in commercial CMOS switches exhibiting charge injection below 20 pC; 2) an upgraded experimental test bench enabling thermal testing of CMOS switches through a modified carrier board design; and 3) detailed analysis of the uncertainty contributions across different charge injection ranges. The revised experimental setup specifically targets precise charge injection characterization in packaged CMOS devices under temperature-controlled conditions.

This work is motivated by the growing demand for high-precision electrical measurements, driven both by fundamental scientific research and by industries such as automotive, aerospace, healthcare, and energy. Although precision ADCs with resolutions beyond 16 bits are essential for high-accuracy waveform digitizers, they remain inadequate to replace conventional thermal converters or to cover the full frequency range required in ac electrical metrology. To address this gap, several National Metrology Institutes (NMIs) are investigating the integration of quantum reference standards—particularly Josephson voltage standards—with ADCs, for establishing a direct link of ac quantities to the revised International System of Units (SI) [13], [14], [15]. Novel ADC architectures with performance exceeding that of current commercial solutions are required to achieve this goal.

II. Charge Injection Phenomena in Analog CMOS Switches: Review and Modeling

A circuit demonstrating the concept of a basic T/H configuration, utilizing a CMOS switch and a hold capacitor, C_H, is presented in Fig. 1.

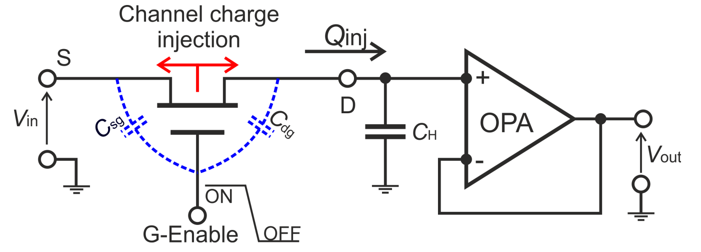

Fig. 1. Simplified T/H circuit. When the switch is turned on, the voltage on the capacitor tracks the input signal; instead, when the switch is turned off, the capacitor holds its value until the switch is turned on again. Intrinsic channel charge injection mechanisms are shown in red. The feedthrough effect is represented by the gate-to-diffusion overlap capacitance, C_{sg} and C_{dg}. Total charge injected by both mechanisms is denoted as Q_{Inj}.

For the following discussion, it is helpful to model the CMOS switch as a nonideal component that exhibits residual leakage resistance and parasitic capacitance, which give rise to voltage errors. Fig. 1 illustrates the charge injection mechanisms in a CMOS switch, that is, intrinsic channel charge injection and clock feedthrough effect. The total injected charge, Q_{Inj}, introduces a pedestal voltage error on the hold capacitor, C_H, when the switch turns off. The pedestal voltage error directly affects the accuracy of high-precision ADCs. Its magnitude is typically in the millivolt range and depends on several factors, including the gate voltage swing during switching and the values of C_{dg} and C_H. Smaller C_H leads to a larger pedestal error. Accurate modeling of the charge injection effect is crucial for high-precision ADC and sample-and-hold circuit design.

The pedestal voltage error due to charge injection, following [2], can be written as

$$\Delta V = (V_G - V_{in}) \frac{C_{dg}}{C_H} \tag{1}$$

where V_G is the voltage control applied to the gate, which is considered to change extremely fast and V_{in} is the input signal at the source. Furthermore, C_{dg} is a semiconductor capacitance that should be minimized, as its voltage dependence introduces nonlinearity.

Moreover, if the injected charge Q_{Inj} remains constant over the input voltage range, it introduces an output offset. A linear variation of Q_{Inj} with the input causes a gain error, while nonlinear dependence leads to distortion and output nonlinearity. For simplicity, the total charge injection is modeled as an overlap capacitor, C_{dg}, since the resulting voltage disturbances are important for the subsequent discussion.

A. Modeling the Effect of Charge Injection

One of the goals of the True8DIGIT project is to evaluate and characterize commercial CMOS switches. Based on the characterization results, switches with best-in-class performance will be selected for potential integration into novel amplifiers, specifically COPAs, for use in integrator and front-end digitizer circuitry. Consequently, understanding and modeling the error sources introduced by the CMOS switches is fundamental to meeting the project's requirements. The key electrical parameter characterized in this work is

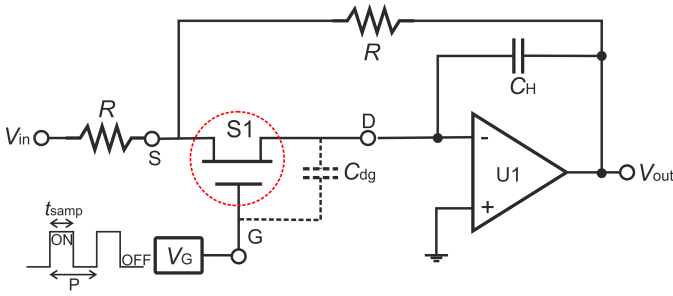

Fig. 2. Conventional closed-loop T/H architecture. The primary objective of this simulation is to analyze the effect of charge injection, modeled by the drain–gate overlap capacitance C_{dg}, on the integrator circuit. For simplicity, the effect of charge injection, modeled by source–gate overlap capacitance C_{sg}, is not shown in the schematic, as its impact on the integrator input is considered negligible.

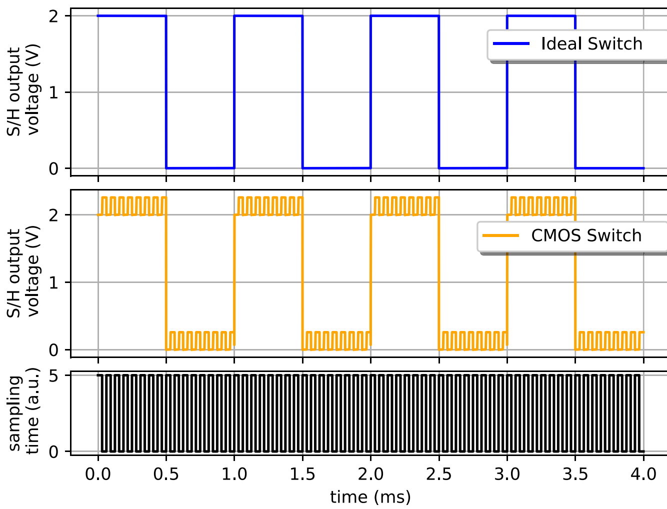

Fig. 3. Simulation of the charge injection effect in a T/H circuit. The top plot shows the T/H hold output when using an ideal switch (C_{dg} = 0); the middle plot shows the charge injection effect (pedestal voltages) on the T/H output when using a realistic CMOS switch with C_{dg}/C_H = 0.1. Simulation parameters were V_{in} = 2 V and V_G frequency of 8 kHz.

charge injection. Our discussion will focus on identifying a suitable model and, based on experimental results, simulating the impact of charge injection on a COPA design utilizing the selected CMOS switches. Nevertheless, it is worth noting that improved T/H designs and circuits are reported in literature [2], [16], aiming to minimize various sources of errors by: 1) reducing the feedthrough error in the hold mode; 2) ensuring constant pedestal error independent of the input voltage; and 3) mitigating pedestal voltage error through compensating techniques.

B. Charge Injection Simulation in a T/H Circuit

A simulation on a conventional closed-loop T/H circuit [2], [16] (see Fig. 2) was performed.

The switch, S_1, is opened and closed at half period of the sampling time, t_{samp}. During switching, charge is injected into the summing node (negative input of U1), adding an extra charge to the hold capacitor C_H. This causes an unwanted pedestal voltage at the output, V_{out}, in addition to the input voltage. This effect is shown in Fig. 3, which compares the

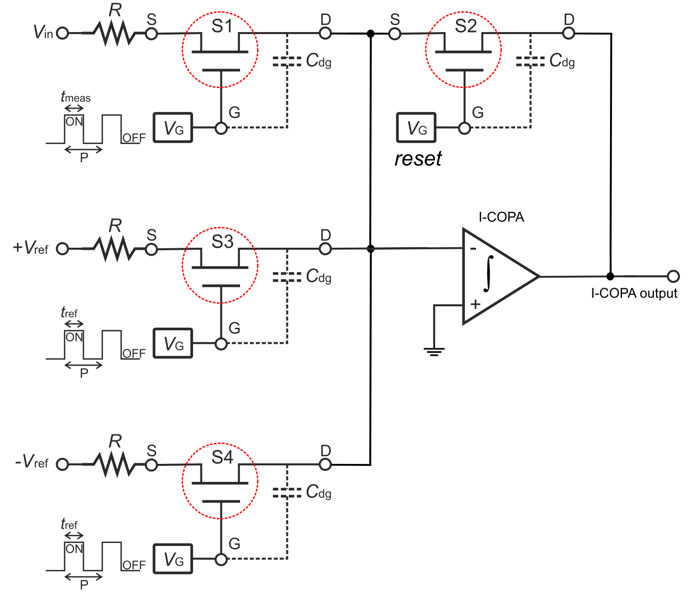

Fig. 4. I-COPA model with four CMOS switches to study the effect of charge injection on its output signal. I-COPA consists of a 3-stage composite amplifier with an integrating capacitor, C_{INT} = 100 pF.

results with those obtained using ideal switches. The pedestal voltage results is $\Delta V \approx 300.0$ mV when S_1 is switched at a sampling rate of 8 kHz with a V_G = 5 V, the input signal used was a square wave with amplitude V_{in} = 2 V peak of frequency 1 kHz and C_{dg}/C_H = 0.1. The pedestal voltage follows the sampling rate as shown at high and low levels of T/H output voltage in the plot at the center of Fig. 3. The simulation was performed during 4 ms time, which encompassed four periods of the input signal.

The closed-loop T/H architecture is preferable in T/H circuits because output errors are minimized due to node D being held at a virtual ground potential.

C. Charge Injection Simulation in I-COPA

Fig. 4 shows a proof-of-concept model/schematic of an integrator composite operational amplifier (I-COPA), being developed within the project [17], used to simulate the impact of charge injection generated by CMOS switches on the output voltage. The I-COPA circuit operates by integrating the input signal at its input port. It is based on a three-stage composite amplifier with an integrating capacitor C_H = 100 pF, selected to maintain a C_{dg}/C_H = 0.1 ratio similar to that used in the T/H simulation. The sequence starts with the reset switch S_2 closed for half a period of the sampling clock. After this time, S_2 remains open until the integrating sequence begins. Then, the switch S_1 is closed, applying the input signal, V_{in}, to the I-COPA input for a constant number of periods of the sampling clock. After that, S_1 is opened, and the I-COPA starts to integrate the voltage reference V_{ref}, with switches S_3 and S_4 closed and opened, respectively, until the I-COPA output voltage reaches 0 V. The integrating sequence then restarts.

The simulation results of the integrator output voltage, when using ideal switches and CMOS switches on the input signal path, are depicted in Fig. 5, where a voltage deviation of up

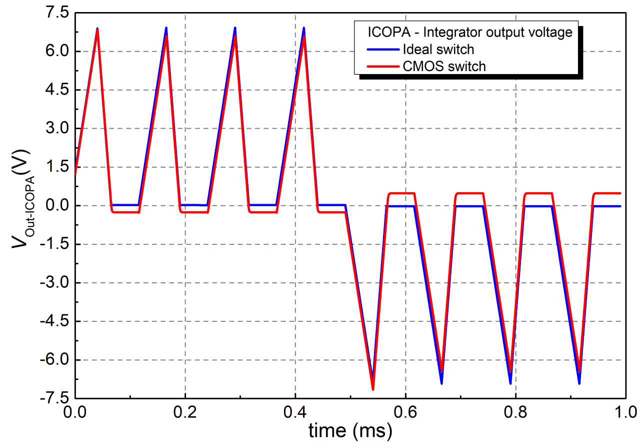

Fig. 5. Results from the simulation of the I-COPA using ideal and realistic CMOS switches. As a consequence of the injected charge, a voltage deviation up to 500 mV appears when using CMOS switches.

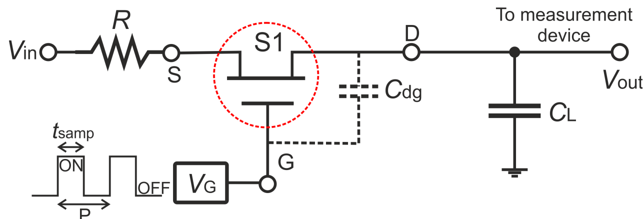

Fig. 6. Schematic of the typical experimental setup for charge injection measurements. C_L is the load capacitor used to determine the charge injection via pedestal voltage measurement.

to 500 mV between the two signals can be observed. The simulated input signal was a square wave with a peak of 2.5 V and a frequency of 1 kHz, sampled at 8 samples/period.

III. Experimental Setup for Charge Injection Measurement in Silicon-Gate CMOS-Based Switches

To mitigate such errors, accurate switch selection is necessary. The most common approach to experimentally measuring charge injection in CMOS switches involves loading the switch with a large capacitance, C_L, typically around 1 nF, as illustrated in Fig. 6.

A similar setup for the accurate and traceable measurement of charge injection in CMOS switches has been implemented at INRiM and is schematically depicted in Fig. 7.

It is composed as follows.

1) DUT CMOS is the device to be characterized. Different devices have been tested [19], [20], [21], [22]: all the devices exhibit on-channel resistance R_{on} ranging from 1.8 to 90 Ω at 25 °C and leakage currents typically in the range 20–30 pA. Break-before-make (BBM) switching action is implemented in all the DUTs identified, having a typical time delay interval ranging from 10 to 30 ns.
2) DC-voltage calibrator Fluke 5730A[1] has been selected in this work for its high precision, long time stability, and very low drift, lower than 5μV/V. Below 10 V, the calibrator is traceable to the INRiM primary dc voltage standard [23].
3) C_S is a standard capacitor, which is part of a set of decadic air–dielectric capacitors Agilent 16380A series (1 , 10 , 100 , and 1000 pF). Each standard capacitor was calibrated against the Italian national standard of capacitance at 1 kHz using a capacitance-loss bridge Andeen-Hagerling AH2700.
4) DMM is a digital multimeter, Keysight 3458A, operated in the DCV digitizing mode, with a sampling frequency of 100 kHz and an aperture time of 1.4 μs, thus achieving a 16-bit resolution. A simplified input impedance circuit is schematically represented in Fig. 7, where C_{IN}, R_{IN}, and I_b represent the input capacitance, resistance, and bias current, respectively, of the input circuitry of the IADC of the DMM. The capacitors C_{Guard} and C_{Gnd} represent the capacitive coupling between the IADC and the internal DMM guard, as well as the capacitive coupling between the internal DMM guard and its chassis, which is always connected to the mains earth. The DMM gain error in the employed digitizing mode has been measured using a dc Josephson voltage standard.
5) AWG is an HP33120A arbitrary waveform generator used to synthesize a TTL-like signal with amplitude V_{IN} to control the ON–OFF switching of the DUTs. Its synchronous trigger output is used to trigger the acquisition process.
6) APS is a programmable dual analog power supply used to provide the necessary positive and negative voltage reference, V_{CC} and V_{EE}, for all DUTs, according to the specifications provided by the manufacturers.
7) R is a standard resistor, which could be manually connected in series to the source port, S of the DUTs. When R is not inserted, the DUT is tested in the *voltage* mode, whereas when R is inserted, the DUT is tested in *current-steering* mode. The presented results refer only to voltage mode operation.

A photograph of the measurement setup is shown in Fig. 8.

An important consideration when using digital multimeters in conjunction with a standard capacitor to measure small electrical charges is the initial evaluation and identification of potential systematic errors within the experimental setup. It is well established that both the input parameters of the DMM and other "leakages" within the experimental setup can influence the final accuracy of the measured electrical quantity, thus leading to systematic errors. Section IV presents a novel measurement method suitable for determining both charge injection and parasitic capacitance of the experimental setup.

IV. Measurement Method, Results, and Discussion

According to the simulation circuit in Fig. 6 and the measurement setup in Fig. 7, the measurement model to determine the switch charge injection can be written as

$$Q_{Inj} = \Delta V\, C_L = \Delta V\, (C_S + C_P) \tag{2}$$

[1]Brand names are used for identification purposes, and such use implies neither endorsement by the authors nor assurance that the equipment is the best available in the market.

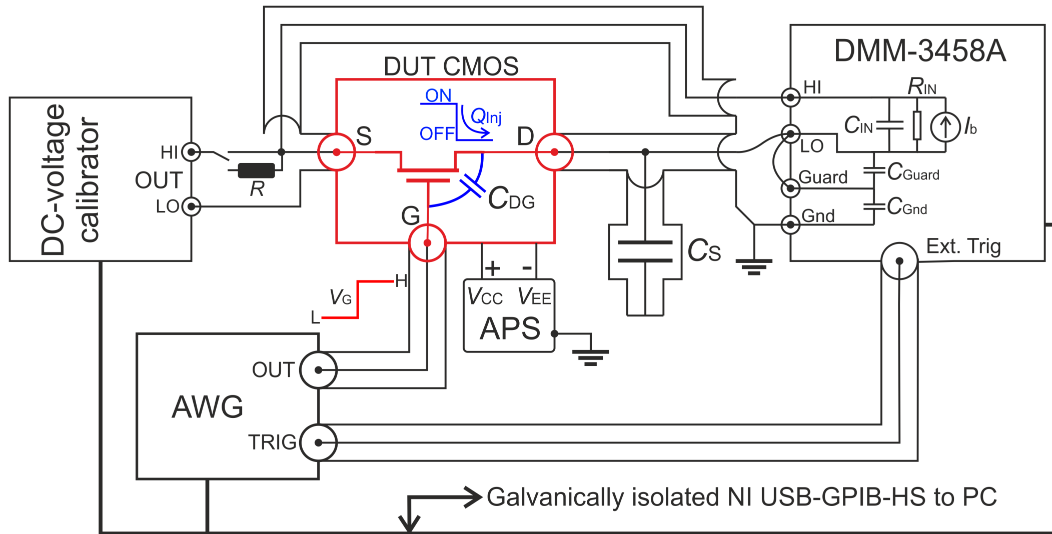

Fig. 7. Schematic of the experimental setup employed for traceable charge injection measurements in CMOS switches.

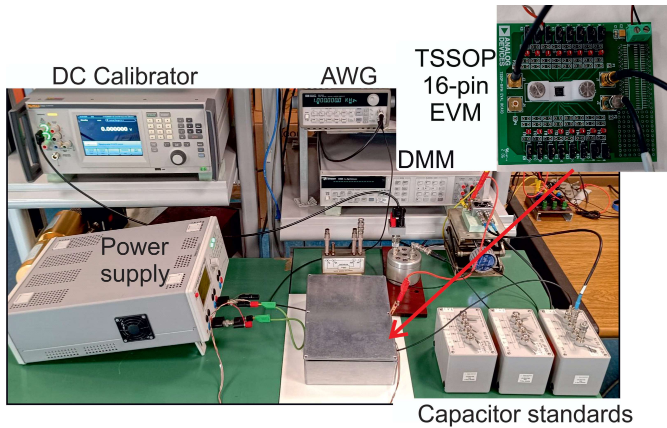

Fig. 8. Photograph of the experimental setup. The capacitor standards shown are part of the Agilent 16380A series. The CMOS switches under test are installed on commercial evaluation boards.

where ΔV is the voltage difference measured by the DMM in the digitizing mode, C_L is the load capacitance, composed of both a calibrated standard capacitor, C_S, and an unknown parasitic capacitance, C_P, which includes the DMM input impedance,[2] cables, connectors, and carrier board. For accurate charge injection measurements, the effect of C_P must be taken into account. For this purpose, a new method has been developed, tested, and compared with other methods reported in literature [24], [25].

TABLE I

SIMULATION PARAMETERS FOR THE ADG1413 AND ONSEMI MC74LVX4053 SWITCHES

Channel	Condition	t_{ox} / nm	W/L	V_{th} / V
ADG1413				
N	Initial	100	1170/2	0.7
	Final	3	2170/2.55	0.7
P	Initial	100	1700/2	-0.7
	Final	8	2278/2.55	-0.9
Onsemi MC74LVX4053				
N	Initial	14	2170/0.79	0.7
	Final	14	2170/0.79	0.9
P	Initial	14	2278/0.79	-0.9
	Final	14	2278/0.79	-0.9

The method presented here uses a set of three calibrated capacitor standards, C_S, with nominal values of 10 , 100 , and 1000 pF. For each C_S, the corresponding pedestal voltage ΔV due to Q_{Inj} is determined. The switch control frequency provided by the AWG was set to 1 kHz, so that the capacitor discharge effect when the switch is open is reduced, and the output voltage resembles a square wave. As depicted in Fig. 7, the high and low input terminals of the DMM are connected in a differential configuration, allowing the difference between the drain and source voltages to be sampled. This setup enables the DMM to operate within the 1 V range, thus preserving high vertical resolution for all the measurements.

For each dc voltage V_{in} supplied by the calibrator, the CMOS switch is turned on and off by applying to its gate terminal a TTL-like signal provided by the AWG. The resulting change in the output voltage is digitized by the DMM over a period of 1 s (Fig. 9). A processing algorithm developed in *MATLAB* automatically computes the pedestal voltage ΔV at each transition and performs a statistical analysis.

As shown in (2), the pedestal voltage, ΔV, is inversely proportional to the load capacitance, C_L. By performing a linear regression analysis on the three (C_S, $1/\Delta V$) pairs, the charge injection, Q_{Inj}, and its uncertainty are estimated.

[2]As shown in Fig. 7, the DMM input model includes the bias current I_b. From the DMM-3458A specifications, this current is ≤20 pA at 25 °C. In the worst case, if all of the I_b flows through C_{DS} and C_S = 10 pF, the offset voltage, considering the measurement timescale of 1 ms, would be $\Delta V = (I_b/C_S) \cdot \Delta t \approx 2$ mV. In practice, part of I_b also flows into the output terminal of the dc-calibrator (Fluke 5730A), which provides a very low-impedance path to ground. A simple current divider model between the calibrator output impedance and the reactance of C_S ($|Z_{C_S}| \approx 16$ MΩ at 1 kHz) shows that only a tiny fraction of the current charges C_S, reducing the offset to the sub-μV range. This contribution is, therefore, negligible compared to the millivolt-level charge-injection signals measured (see Fig. 9).

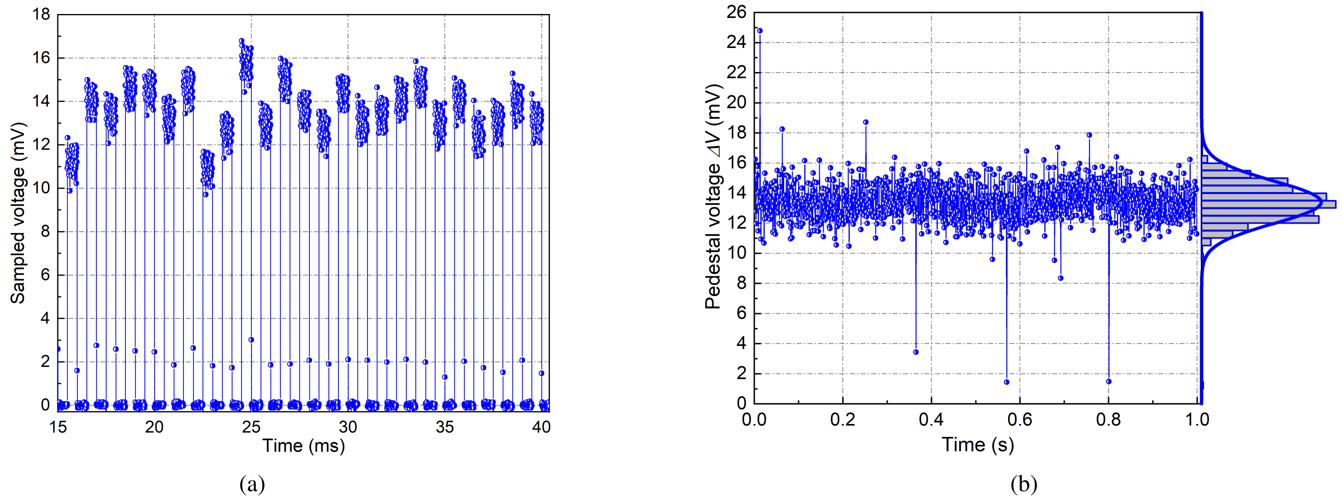

Fig. 9. Measurement results for the ADG1413 switch operating in dual-supply mode (V_{CC} = 15 V, V_{EE} = −15 V), with V_{in} = 1 V, C_S = 10 pF and 1 kHz gate control signal V_G. (a) Portion of the almost-rectangular digitized voltage signal due to the charge injection effect having 1 ms period. (b) Pedestal voltage data points reconstructed from the total sampled voltage measurements using a 1-s measurement window, which approximately follows a normal distribution.

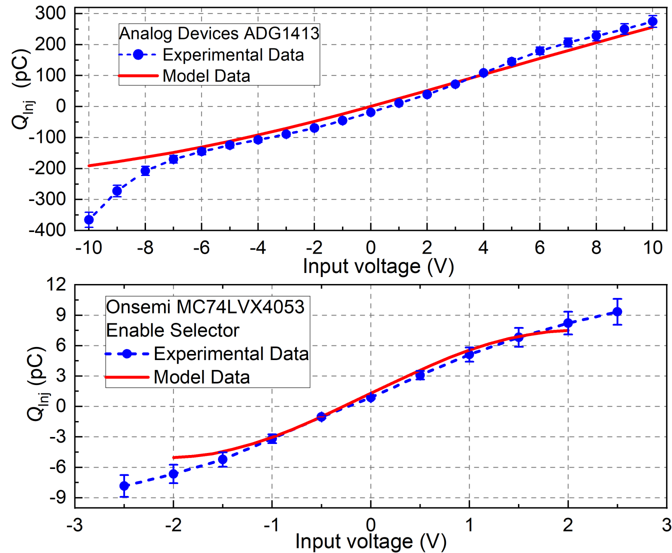

Fig. 10. Charge injection Q_{Inj} measurement and simulation results for: 1) high-Q_{Inj} switch Analog Devices ADG1413, which is a monolithic device containing four independently selectable switches [19], and 2) low-Q_{Inj} switch Onsemi MC74LVX4053, a high-performance analog multiplexer/demultiplexer [20]. Simulation results on both devices are depicted in red. Uncertainty bars represent expanded uncertainty with a coverage factor of (k = 2).

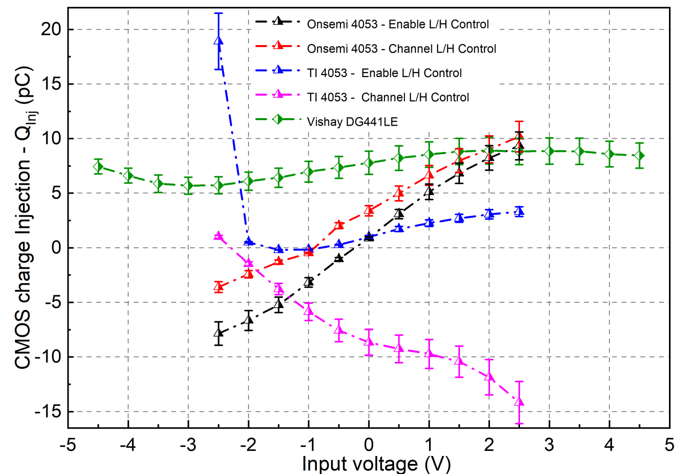

Fig. 11. Experimental results for three low-Q_{Inj} CMOS switches: Onsemi 4053 and Texas Instruments 4053 in both "Enable" and "Address/Channel selector" control modes (dual-supply mode V_{CC} = 3 V, V_{EE} = −3 V); Vishay DG441LE switch (dual-supply mode V_{CC} = 5 V, V_{EE} = −5 V). Uncertainty bars represent expanded uncertainty with a coverage factor of (k = 2).

Furthermore, a switch computer model was developed in LTSpice based on the experimental data, employing a complementary nMOS/pMOS transistor pair connected in parallel. Key parameters of the model, including the channel width-to-length ratio (W/L), the zero-bias threshold voltage V_{th}, and the gate oxide thickness t_{ox}, were adjusted according to standard values from typical CMOS fabrication processes. Initial and final parameters for Analog Devices ADG1413 and Onsemi MC74LVX4053 switches are reported in Table I.

Measurement and simulation results of the injected charge Q_{Inj} for the Analog Devices ADG1413 [19] switch, corresponding to input voltages V_{in} ranging from −10 to 10 V, are shown in Fig. 10 (top), revealing a relatively large charge injection even at low input voltages (approximately 50 pC at 2 V). As shown in the plot, the simulated curve exhibits good overall agreement with the experimental measurements, although some discrepancies remain, particularly near the negative edge of the input voltage range, suggesting that further model refinement may be beneficial. Moreover, Fig. 10 (bottom) presents the measurement and simulation results for the Onsemi MC74LVX4053. To this end, the SPICE model employed in the ADG1413 simulation was specifically retuned. The revised model agrees well with the experimental data in the central portion of the input voltage range. However, as the input voltage nears the supply rails, saturation effects in the CMOS transistors become increasingly pronounced.

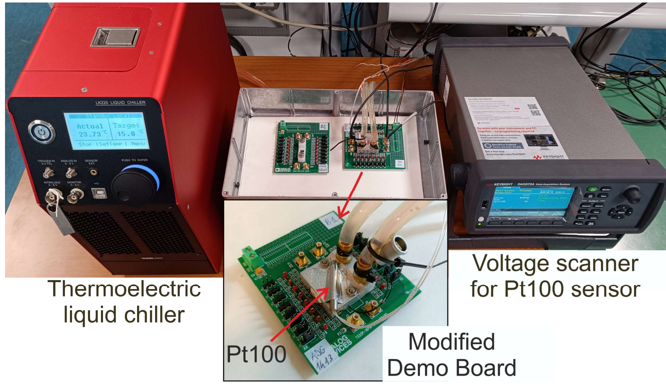

Fig. 12. Experimental setup for charge injection measurement at different temperatures. The external Pt100 temperature sensor is mounted directly onto the metal package used to thermalize the CMOS switch.

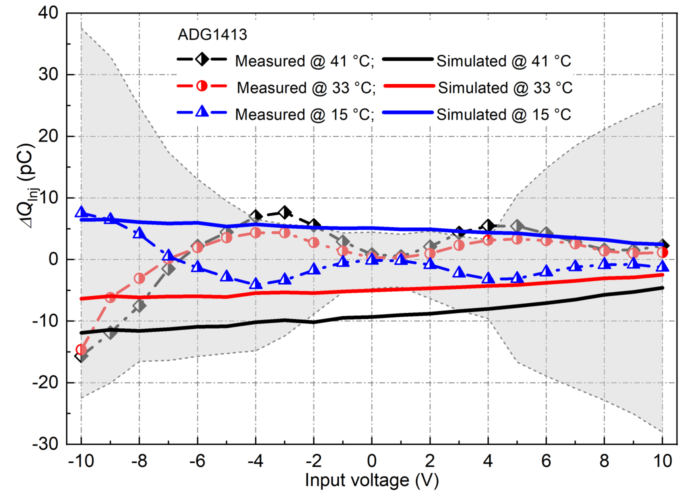

Fig. 13. Measurement and simulation results of charge injection differences $\Delta Q_{\mathrm{Inj}}(T)$, for the ADG1413 switch, at different temperature setpoints T, with respect to reference temperature, $T_{\mathrm{Ref}} = 24$ °C. The shaded area represents the expanded uncertainty with a coverage factor of ($k = 2$), calculated via propagation of uncertainty for the $\Delta Q_{\mathrm{Inj}}(T)$ quantity. For clarity, the uncertainty is shown only for the experimental data measured at 15 °C (blue symbols).

Further experimental results for low-Q_{Inj} CMOS switches are illustrated in Fig. 11 for input voltages V_{in} between −5.0 and 5.0 V.

As specified in both Onsemi and Texas Instruments 4053 model datasheets [20], [21], the digital control signal V_{G} can be applied either to the "Enable" pin or to the "Address/Channel selector" pin corresponding to the specific channel being used. In the first case, all three on-chip channels are simultaneously disabled, whereas by digitally controlling the address selector, each channel can be operated independently.

Measurement results for the Onsemi 4053 series CMOS switches show charge injection values within ±10 pC across the tested input voltage range, in both operating modes, with an approximately linear dependence on input voltage. In contrast, the Vishay DG441LE switch exhibits slightly higher charge injection levels, though they remain nearly constant over the same voltage range. The evaluation of measurement uncertainty is presented in Section V.

The measured charge injection values for all CMOS switches are consistent with the manufacturer's specifications. It is worth noting that, in the Vishay CMOS chip [22], the charge injection curve is entirely positive and nearly constant. This behavior is likely due to its asymmetric internal design and compensation circuitry, made of PMOS and NMOS transistors purposely designed and arranged to yield an output voltage error almost independent of input voltage.

A. Impact of Temperature on CMOS Charge Injection: Experimental and Simulation Insights

The experimental setup described in Section IV was upgraded with a new facility designed to evaluate the temperature dependence of CMOS charge injection: a second evaluation board, used for CMOS switch characterization, was modified and enhanced to support this measurement campaign. Specifically, the upper section of the demo board hosting the CMOS chips was replaced with a metal block containing an internal cavity, within which a temperature-controlled liquid circulates. This liquid is precisely regulated using a commercial thermoelectric chiller.

The chiller's internal temperature can be controlled using either an internal or an external temperature sensor. During the initial experiment, excessive noise was observed, attributed to capacitive coupling between the external temperature sensor and the metal block. To mitigate this, the external sensor was removed, and a second temperature sensor was installed directly onto the metal block, enabling real-time monitoring via a voltage scanner, while the chiller continued regulating the liquid temperature using its internal sensor. Fig. 12 shows a photograph of the experimental setup.

Additionally, a simulation was performed to investigate the temperature dependence of charge injection by varying the temperature in the simulated LTSpice switch model from 15 °C to 41 °C. The comparison between the measurement and simulation results for the ADG1413 switch—which exhibited the largest temperature variation in charge injection—is shown in Fig. 13. The graph displays the absolute difference in charge injection computed as $\Delta Q_{\mathrm{Inj}} = Q_{\mathrm{Inj}}(T) - Q_{\mathrm{Inj}}(T_{\mathrm{Ref}})$, where $Q_{\mathrm{Inj}}(T)$ represents the charge injection measured at a given temperatures, T, and $Q_{\mathrm{Inj}}(T_{\mathrm{Ref}})$ represents the charge injection measured at a reference temperature, T_{Ref}, fixed approximately to 24 °C. As shown in the graph, the maximum ΔQ_{Inj} measured was about 23 pC, corresponding to a temperature variation $\Delta T = 26$ °C for −10 V input voltage. The measurement and simulation results agree well within the measurement uncertainties.

V. Measurement Uncertainty Assessment

As mentioned in Section IV, the amount of charge injection was computed using a postprocessing technique based on linear regression analysis. The set of calibrated standard capacitors, $C_{\mathrm{S}} = \{C_1, C_2, C_3\}$, was used to measure the corresponding reciprocal pedestal voltages, $1/(\Delta V) =$

$\{1/(\Delta V_1), 1/(\Delta V_2), 1/(\Delta V_3)\}$, following the method described in Section IV. By transforming (2) to its linear representation

$$C_S = \frac{1}{\Delta V} \cdot Q_{Inj} - C_P \quad (3)$$

it was possible to evaluate the slope of the best-fit line, which corresponds to the charge injection Q_{Inj}. The intercept of the best-fit line, corresponding to C_P, accounts for parasitic capacitance effects.

The measurement uncertainty associated with the postprocessing method was computed using the orthogonal distance regression (ODR) algorithm [26], that minimizes the orthogonal distances between the measured data points and the best-fit curve, taking into account the uncertainties in both independent and dependent variables, that is, $u(C_S)$ and $u(1/(\Delta V))$, respectively. Similar to ordinary least-squares (OLS) methods, ODR uses the model's Jacobian along with a weighting matrix derived from measurement uncertainties to calculate parameter covariance. Unlike OLS, however, ODR also corrects for the independent variables within the fitting process, so that measurement errors in x are considered along with those in y, and both are propagated consistently across parameter uncertainties. Further details can be found in the ODRPACK guide in [26].

The estimation of input uncertainties $u(C_S)$ and $u(\Delta V)$ has been performed as follows.

1) The value of the air–dielectric capacitors is computed according to the following equation:

$$C_S = C_S^{Cal} + \delta C_D + \delta C_T + \delta C_{ac-dc} \quad (4)$$

where

C_S^{Cal} calibration value of the air–dielectric capacitors;

δC_D correction due to the capacitance temporal drift;

δC_T correction due to the temperature coefficient;

δC_{ac-dc} correction for the ac–dc capacitance difference in air–dielectric capacitors [27], since the capacitors during calibration are excited using a sine wave, whereas in the present experiment they are excited with a quasirectangular voltage profile.

The total standard uncertainty of air–dielectric capacitors $u(C_S)$ is then calculated using the following equation:

$$u^2(C_S) = u^2\left(C_S^{Cal}\right) + u^2(\delta C_D) + u^2(\delta C_T) + u^2(\delta C_{ac-dc}) \quad (5)$$

2) Similarly, the pedestal voltage measurement ΔV, from which the reciprocal pedestal voltage used in the linear relation (2) is derived, can be mathematically modeled as follows:

$$\Delta V = \overline{V_{DMM}} + \delta V_{DMM}^{G} + \delta V_{DMM}^{NL} + \delta V_{DMM}^{RES} + \delta V_{DMM}^{\tau} \quad (6)$$

where

$\overline{V_{DMM}}$ measured pedestal voltage, determined from repeated measurements, with its relative uncertainty evaluated using statistical methods (Type A uncertainty);

δV_{DMM}^{G} gain correction of the digitizer, its relative uncertainty in sampling mode has been evaluated by means of a dc Josephson voltage standard and a Fluke 5730A calibrator;

δV_{DMM}^{NL} correction for the digitizer nonlinearities;

δV_{DMM}^{RES} correction for the digitizer resolution;

δV_{DMM}^{τ} correction for possible voltage decay during the measurement of the pedestal voltage measurement with the capacitor in the hold mode.

The digitizer offset voltage does not contribute to measurement uncertainty because the processing algorithm (Section IV) evaluates ΔV as the difference between the high and low levels of the rectangular waveform [see Fig. 9(a)]. Any constant offset present in the digitizer cancels out in this difference, making its effect negligible. Furthermore, the contribution from the bias current of the DMM has not been considered, as it is estimated to be in the sub- μV range and is therefore negligible for these measurements.

Therefore, the total standard uncertainty of the pedestal voltage $u(\Delta V)$ is obtained from the following equation:

$$u^2(\Delta V) = u^2\left(\overline{V_{DMM}}\right) + u^2\left(\delta V_{DMM}^{G}\right) + u^2\left(\delta V_{DMM}^{NL}\right) + u^2\left(\delta V_{DMM}^{RES}\right) + u^2\left(\delta V_{DMM}^{\tau}\right). \quad (7)$$

Table II presents the uncertainty budget for various charge injection measurements, ranging from a few pC to hundreds of pC, evaluated on various CMOS switches selected in the present work.

A. Discussion on the Charge Injection Uncertainty Budget

To assess the influence of each uncertainty contribution to the overall charge injection uncertainty, $u(Q_{Inj})$, each input uncertainty, $u(x_i)$, appearing in Table II, was sequentially set to zero while all other uncertainties were maintained at their predefined values. The ODR algorithm was run again to calculate the resulting charge injection uncertainty. The effect of the single uncertainty contribution $u_i(Q_{Inj})$ was then computed from

$$u_i^2\left(Q_{Inj}\right) \simeq u^2\left(Q_{Inj}\right) - u_{u(x_i)=0}^2\left(Q_{Inj}\right) \quad (8)$$

where

$u(Q_{Inj})$ is the ODR-estimated charge injection uncertainty with all the uncertainty contributions in (5) and (7) and

$u_{u(x_i)=0}(Q_{Inj})$ is the ODR-estimated charge injection uncertainty with $u(x_i)$ input uncertainty contribution set to zero.

Furthermore, as shown in Table II, the uncertainty in measuring charge injection with the standard set of air–dielectric

TABLE II

EXAMPLE UNCERTAINTY BUDGET OF CHARGE INJECTION Q_{Inj} MEASURED ON DIFFERENT CMOS SWITCHES AT DIFFERENT RANGES. ALL THE UNCERTAINTIES COMPONENTS ARE EXPRESSED IN RELATIVE TERMS WITH RESPECT TO THE MEASURED CHARGE AS PERCENTAGE, $u_i(Q_{\mathrm{Inj}})/Q_{\mathrm{Inj}}$

	$u_i(Q_{\mathrm{Inj}})/Q_{\mathrm{Inj}}$ (%)	
Uncertainty source $u(x_i)$	$1\,\mathrm{pC} \lesssim Q_{\mathrm{Inj}} < 30\,\mathrm{pC}$	$30\,\mathrm{pC} \lesssim Q_{\mathrm{Inj}} < 350\,\mathrm{pC}$
C_{S} : Standard capacitance		
Calibration @ 1 kHz (Type B)	0.011 – 0.001	0.002 – 0.002
Temperature effect (Type B)	0.011 – 0.001	0.002 – 0.002
Time drift (Type B)	0.009 – 0.004	0.004 – 0.004
AC-DC relative difference (Type B)	0.013 – 0.009	0.011 – 0.011
ΔV : Pedestal voltage measurement		
Repeatability @ 1 s (Type A)	1.583 – 0.329	0.091 – 0.011
Digitizer gain (Type B)	0.002 – 0.001	0.001 – 0.001
Digitizer non-linearity (Type B)	10.95 – 1.187	0.313 – 0.030
Digitizer resolution (16 bit) (Type B)	3.709 – 0.398	0.112 – 0.011
Capacitor discharge time (τ) (Type B)	0.215 – 0.230	0.130 – 0.088
Combined standard uncertainty $u(Q_{\mathrm{Inj}})$	11.67 – 1.315	0.368 – 0.095
Goodness of statistical fit χ^2_ν	0.342 – 0.008	2.084 – 1319
Scaled combined standard uncertainty $u_{\mathrm{s}}(Q_{\mathrm{Inj}})/Q_{\mathrm{Inj}} = \sqrt{\chi^2_\nu} \cdot u(Q_{\mathrm{Inj}})/Q_{\mathrm{Inj}}$	6.820 – 0.118	0.532 – 3.446

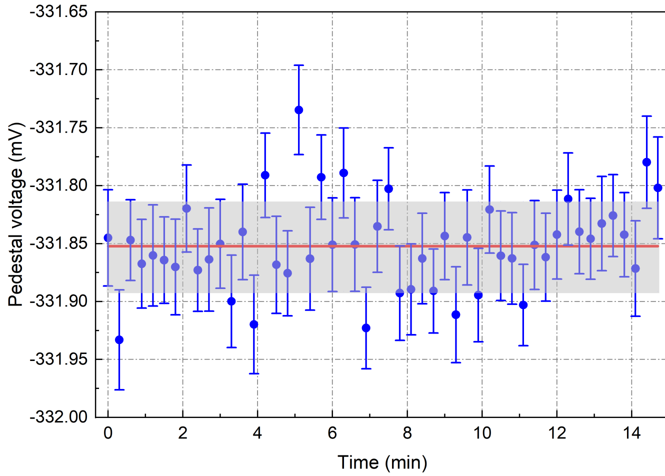

Fig. 14. Repeated measurements of the pedestal voltage ΔV across the C_{S} = 10 pF standard capacitor for the ADG1413 switch at $Q_{\mathrm{Inj}} \simeq 100$ pC over a period of 15 min. Error bars represent the Type A uncertainty of every single measurement (1 s). The horizontal red line and gray-shaded area represent the mean and standard deviation of the data, respectively.

capacitors is negligible compared to that arising from the pedestal voltage measurements ΔV. The dominant source of the uncertainty in ΔV is the digitizer nonlinearity error, estimated 100 μV for a sampling rate of 100 kS/s, an aperture time of t_{a} = 1.4 μs and a 1 V input range [28]. This effect is particularly significant when measuring low charge injection values ($Q_{\mathrm{inj}} \lesssim 3$ pC)) with the 1000 pF capacitor as the charge detector, where the voltage amplitude is greatly reduced.

The remaining DMM-related uncertainty contributions are estimated as follows: $\delta V^{\mathrm{G}}_{\mathrm{DMM}}$ about 10 μV/V; $\delta V^{\mathrm{RES}}_{\mathrm{DMM}}$ about 17 μV, from the least significant bit (LSB); $\delta V^{\tau}_{\mathrm{DMM}}$ below 1 mV, based on worst case measurements ($Q_{\mathrm{inj}} \sim 350$ pC and C_{S} = 10 pF). The digitizer input range was fixed at 1 V, sufficient to cover nearly all pedestal voltages generated by the CMOS switches using the same set of air–dielectric capacitors. In principle, DMM sampling uncertainties could be further reduced by modeling range-dependent effects (gain, nonlinearity, and resolution), though at the cost of greater model complexity. Furthermore, it was observed that as Q_{Inj} increases, the experimental data progressively deviate from the linear relationship described by (3). This suggests that further systematic effects or refined measurement models might be considered.

The statistical parameter that accounts for the goodness of fit is the reduced chi-square parameter (χ^2_ν): a value of $\chi^2_\nu \approx 1$ indicates that the model's predictions are consistent with the observed data and that the uncertainties are well estimated; $\chi^2_\nu \ll 1$ suggests that the uncertainties may be overestimated, while $\chi^2_\nu \gg 1$ indicates that the model may not be suitable for the data or that the uncertainties are underestimated.

To account for possible model inadequacy as well as uncertainty overestimation, the combined standard uncertainty $u(Q_{\mathrm{Inj}})$ has been purposely rescaled by a factor of $\sqrt{\chi^2_\nu}$, making it the dominant contribution to the final uncertainty for charge injection values above 50 pC.

Table II summarizes all uncertainty contributions arising from the capacitance standards, pedestal voltage measurements, and the ODR fit used to calculate the charge injection and its relative uncertainty, along with the goodness of statistical fit expressed in terms of the reduced chi-square parameter.

Further tests were conducted to identify and quantify possible influences of the measurement setup that could explain the model inadequacy. For example, it is worth noting that each switch characterization was repeated multiple times over

several months, consistently yielding results in agreement across all repetitions. In particular, the Vishay DG441LE showed very good agreement with the linear model ($\chi^2_\nu \lesssim 1$) at $Q_{\mathrm{Inj}} \sim 10$ pC. In contrast, other devices exhibited a larger deviation from the linear model at the same Q_{Inj}, suggesting that this effect may be switch-dependent.

Possible charge injection Q_{Inj} and/or parasitic capacitance C_{P} variation in a time-scale of approximately 15 min has been investigated by performing a repeated pedestal voltage measurement with the ADG1413 switch at $Q_{\mathrm{Inj}} \simeq 100$ pC. Fig. 14 shows the measurement results for the 10 pF standard capacitor. No significant drift of the measured pedestal voltage can be observed, thus indicating that both the charge injection and parasitic capacitance remain stable throughout the entire measurement with the three standard capacitors.

This analysis suggests that deviations from linearity may be device dependent, especially at high Q_{Inj} levels, underscoring the need for further investigation to better characterize the CMOS switches and minimize the absolute uncertainty.

VI. Conclusion

This article presents the key outcomes of the research conducted within the European Partnership on Metrology (EPM) project True8DIGIT, highlighting the development of a novel experimental setup and measurement method for the metrological characterization of charge injection in CMOS switches. A set of commercial CMOS switches has been extensively characterized, and the measurement results have been used to simulate the influence of charge injection effect on the output of a novel I-COPA, which could be integrated in the front-end circuitry of a high-precision digitizer.

The method ensures a resolution lower than 1 pC, which is sufficient for charge injection measurement of best-in-class CMOS switches. The uncertainty analysis shows Type A uncertainties ranging from 10 fC to 70 fC, while Type B contributions increase the overall relative uncertainty to a few percent in the worst case scenario. At low charge injection levels, this is primarily due to digitizer nonlinearities, whereas at higher charge injection values, regression analysis corrections are necessary to account for deviations from the expected linear model. The best relative uncertainties, well below 1%, are achieved around ± 10 pC for CMOS switches that consistently follow the expected linear model.

The investigation of the temperature dependence of charge injection, both experimentally and through modeling, reveals that temperature effects are relatively small. For CMOS switches exhibiting high charge injection, the maximum temperature-induced variation was less than 1 pC/C, with charge injection in the 300 pC range. This effect decreases approximately linearly for lower charge injection values.

The measurement setup, combined with the postprocessing methodology, constitutes a precise and traceable tool for characterizing charge injection in CMOS switches. Further improvements are possible, particularly for charge injection levels below 1 pC. Although the project demands extremely stringent sub-pC limits to achieve true 8.5 digits resolution for an integrating digitizer, best-in-class switches, specified at a few pC and confirmed by our measurements as well, will meet the effective design requirement once appropriate compensation charge injection mitigation techniques are applied or novel switches having sub-pC will be identified and tested.

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References

[1] W. C. Goeke, "An 8 1/2-digit integrating analog-to-digital converter with 16-bit, 100,000 -sample-per-second performance," *Hewlett-Packard J.*, vol. 40, no. 2, p. 3, Apr. 1989.

[2] R. L. Swerlein, "Precision AC voltage measurements using digital sampling techniques," *Hewlett-Packard J.*, vol. 40, no. 2, Apr. 1989.

[3] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2001, pp. 405–423.

[4] M. E. Bierzychudek, R. Iuzzolino, H. Malmbekk, M. Šíra, and B. O. Trinchera, "An SSR-based multiplexer for power measurement," in *Proc. Conf. Precis. Electrom. Meas.*, 2022, pp. 1–2.

[5] B. Trinchera, P. Durandetto, and D. Serazio, "Quantum sampling AC standard for electrical power metrology based on programmable Josephson junction series array," *Measurement*, vol. 233, Jun. 2024, Art. no. 114747, doi: 10.1016/j.measurement.2024.114747.

[6] B. J. Sheu and C. Hu, "Switch-induced error voltage on a switched capacitor," *IEEE J. Solid-State Circuits*, vol. JSSC-19, no. 4, pp. 519–525, Aug. 1984.

[7] G. Wegmann, E. A. Vittoz, and F. Rahali, "Charge injection in analog MOS switches," *IEEE J. Solid-State Circuits*, vol. JSSC-22, no. 6, pp. 1091–1097, Dec. 1987.

[8] J.-H. Shieh, M. Patil, and B. J. Sheu, "Measurement and analysis of charge injection in MOS analog switches," *IEEE J. Solid-State Circuits*, vol. JSSC-22, no. 2, pp. 277–281, Apr. 1987.

[9] B. Sheu, J.-H. Shieh, and M. Patil, "Modeling charge injection in MOS analog switches," *IEEE Trans. Circuits Syst.*, vol. JSSC-34, no. 2, pp. 214–216, Feb. 1987.

[10] A. Danchiv and M. Bodea, "A new simplified model for charge injection induced sample and hold error," in *Proc. Melecon - 15th IEEE Medit. Electrotechnical Conf.*, Apr. 2010, pp. 743–748.

[11] European Partnership on Metrology (EPM). *True8DIGIT Project (22RPT02)*. Accessed: Jul. 11, 2025. [Online]. Available: https://true8digit.eu

[12] B. Trinchera, P. Durandetto, and R. Iuzzolino, "Traceable characterization and simulation of charge injection in CMOS electronic switches," in *Proc. IEEE Int. Instrum. Meas. Technol. Conf. (I2MTC)*, May 2025, pp. 1–6.

[13] A. Rufenacht, C. J. Burroughs, S. P. Benz, P. D. Dresselhaus, B. C. Waltrip, and T. L. Nelson, "Precision differential sampling measurements of low-frequency synthesized sine waves with an AC programmable Josephson voltage standard," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 4, pp. 809–815, Apr. 2009.

[14] J. Lee et al., "An AC quantum voltmeter based on a 10 V programmable Josephson array," *Metrologia*, vol. 50, no. 6, pp. 612–622, Dec. 2013.

[15] L. Palafox, G. Ramm, R. Behr, W. G. Kurten Ihlenfeld, and H. Moser, "Primary AC power standard based on programmable Josephson junction arrays," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 2, pp. 534–537, Apr. 2007.

[16] B. Razavi, *Principles of Data Conversion System Design*. New York, NY, USA: IEEE Press, 1995.

[17] Oliver Power, "True8DIGIT project aims to provide the groundwork for the next generation of precision digitisers," *Electron. World*, vol. 130, no. 2043, pp. 44–45, Feb. 2025. [Online]. Available: https://content.yudu.com/web/69r/0A4417d/EWorldFebruary2025/html/print/Electronics%20World%20February%202025DL.pdf

[18] B. Harvey, "On building physically accurate analog switch macromodels," *Analog Dialogue*, vol. 54, no. 1, pp. 18–29, Jan. 2020.

[19] Analog Devices. *ADG1413*. [Online]. Available: https://www.analog.com/en/products/adg1413.html

[20] ON Semiconductor. *MC74LVX4053*. [Online]. Available: https://www.onsemi.com/products/timing-logic-memory/standard-logic/multiplexers/mc74lvx4053
[21] Texas Instruments. *CD74HC4053*. [Online]. Available: https://www.ti.com/product/CD74HC4053
[22] Vishay Siliconix. *DG441LE*. Accessed: May 26, 2025. [Online]. Available: https://www.vishay.com/docs/76754/dg441le.pdf
[23] P. Durandetto, B. Trinchera, D. Serazio, and E. Enrico, "A 10 v PJVS-based DC voltage realization at INRiM," in *Proc. 26th IMEKO TC4 Int. Symp. 24th Int. Workshop ADC/DAC Modelling Test.*, 2023, pp. 133–137.
[24] O. Gunnarsson, A. Bergman, and K.-E. Rydler, "A method for calibration of partial discharge calibrators," *IEEE Trans. Instrum. Meas.*, vol. 48, no. 2, pp. 453–456, Apr. 1999, doi: 10.1109/19.769625.
[25] I. Lenicek, D. Ilic, and R. Malaric, "Determination of high-resolution digital voltmeter input parameters," *IEEE Trans. Instrum. Meas.*, vol. 57, no. 8, pp. 1685–1688, Aug. 2008, doi: 10.1109/TIM.2008.923786.
[26] P. T. Boggs, R. H. Byrd, J. E. Rogers, and R. B. Schnabel, "User's reference guide for ODRPACK version 2.01 software for weighted orthogonal distance regression," Nat. Inst. Standards Technol., Gaithersburg, MD, USA, Tech. Rep., Jun. 1992.
[27] L. Callegaro, V. D'Elia, and B. Trinchera, "A current source for picoammeter calibration," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 4, pp. 1198–1201, Aug. 2007, doi: 10.1109/TIM.2007.900128.
[28] J. Ireland et al., "A method for using Josephson voltage standards for direct characterization of high performance digitizers to establish AC voltage and current traceability to SI," *Meas. Sci. Technol.*, vol. 34, no. 1, Jan. 2023, Art. no. 015003, doi: 10.1088/1361-6501/ac9542.

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