Design and Implementation of a Resistive MV Voltage Divider

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Design and Implementation of a Resistive HV Voltage Divider

M Modarres, D Giordano, M Zucca, G Crotti

Abstract – *In this paper, a new resistive voltage divider having vertically placed resistors is designed. The simulation results, validated by measurements, show a frequency response where the scale factor and the phase error variation ranges are respectively 2.5 and 4 times better than the ones required by standard IEC 61000-4-7:2002. These results take advantage from a plate connected to the low voltage section and a shield separating the HV part from the LV part of the voltage divider..The maximum scale factor deviation from the rated value is about 2.4% and the maximum phase error is about 22.9 mrad. These very good results have been obtained in a wide frequency range up to 9 kHz, which is quite unusual for resistive dividers.*

Keywords: *Voltage Divider, High voltage, Measurement, FEM modeling, stray capacitance*

I. Introduction

One of the key components of grids with distributed generations (DGs) is represented by power electronic converters. These latter increases significantly harmonic emission spectrum towards higher frequencies correlated with modulation frequency of power switching conversion. Thus, typical harmonic analysis up to 2.5 kHz in many power electronics application requires to be extended up to frequency of 9 kHz, which is the lowest frequency of interest for electromagnetic compatibility (EMC)[1].

In addition, numerous problems related to voltage and current harmonic effects on contemporary power systems are commonly observed nowadays, also in the frequency range 2 kHz − 9 kHz. Levels and spectral content of voltage distortions injected into electric power grids are tending to increase although the threshold levels are defined in numerous regulations. Voltage distortion assessments, especially in medium voltage (MV) grids, are usually based on measurements performed by means of voltage transformers whose transfer ratio, when fed by distorted primary voltage, can be significantly different from the rated one. [1]. Then, resulting evolvement of smart grids strongly depend on on the availability of reliable measurement data for monitoring and control of grid electrical quantities [2], including voltage monitoring.

Previous works done on voltage transformers are mainly focused on low frequencies as they are quite vulnerable to the saturation and non linearity introduced by magnetic cores. Inductive voltage dividers (IVD) are also used mainly in low voltages, low frequencies applications and they are also complex in geometry [3-7]. Capacitive voltage dividers (CVD) could solve the problems of inductive voltage dividers (IVDs) providing higher frequency bandwidth in medium voltage (MV) and high voltage (HV) applications [8-11]. However, CVDs present two main drawbacks. The first one is that it is impossible to measure the DC component injected into a MV smart grid or power network consisting of distributed generation (DG) through CVDs [12] . The second is due to the extra electric charge produced in continuously operating CVDs which can make errors in a short period of time.

Among the possible solutions (VDs) for the measurement in smart grids or power grids, where the voltages are characterized by a high total harmonic distortion (THD) index, a resistive voltage divider (RVD) is cheaper and simpler to be built. Usually RVDs, the most common VDs, are used in low frequency applications, as they show inner stray capacitances that worsen the frequency response by increasing frequency. Moreover, they are quite sensitive to the proximity effect if not properly shielded. However, a suitable shield mostly increases the inner stray capacitances making worse the frequency behavior.

This paper shows how an RVD can be designed with improved frequency response. To this purpose, three different kind of stray capacitances related to the divider structure and their effect on the frequency behavior of the considered RVD will be described. Then, a new vertical configuration of the resistors is introduced. Moreover, the importance of considering the ground modeling is demonstrated by representing both simulation and experimental results. Finally, a new RVD configuration with an added LV middle plate is proposed. The different parameters playing a role in the behavior of the divider are varied in the simulation model in order to optimize the final frequency behavior. The optimized model is thus

realized and the experimental results are compared to simulation results.

II. Initial design of the HV RVD

The representation of a circuit of a general VD is shown in Fig. 1. Each impedance Z_{HV} and Z_{LV} could consist of a series (or/and parallel) of different resistors, and/or inductors, and/or capacitors.

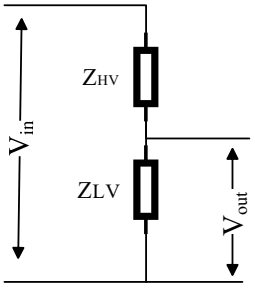


Fig. 1. Schematic of a VD

The two important parameters of a voltage transducer (which includes VDs) are scale factor "*K*" and phase error "$\Delta\varphi$" which can be calculated by using following equations:

$$K = \frac{\left|\overrightarrow{V_{in}}\right|}{\left|\overrightarrow{V_{out}}\right|} = \frac{\left|\overrightarrow{Z_{HV}} + \overrightarrow{Z_{LV}}\right|}{\left|\overrightarrow{Z_{LV}}\right|} \qquad (1)$$

$$\Delta\varphi = \varphi_{out} - \varphi_{in}$$

V_{out} and φ_{out} are the magnitude and phase of the secondary voltage, while V_{in} and φ_{in} identify the primary voltage phasor [13]. The secondary voltage is generally made compatible with the measurement range of the digital acquisition systems and it is commonly between 0V and 5V or 10V. There are many digitizers like National Instruments (NI) cards with nominal voltages in such a range. The nominal voltage of the LV side is considered equal to 5V. Here, it is also worth to mention that digitizers measure the voltage in the upper voltage range if the voltage is more than 80% of that range. For example, if the voltage is about 4V, it is measured in the 5V range. If the voltage is more than 4V, it is measured in the 10 V range.

The rated scale factor (SF) of a divider is defined by the following equation

$$K = \frac{\left|\overrightarrow{V_{in}}\right|}{\left|\overrightarrow{V_{out}}\right|} \qquad (2)$$

Using a VD having a SF approximately equal to 10000, if the input voltage is less than 40000 V, the output voltage will be measured by the range of 5V, while the range 10V will be used for the output measurements when the input voltage is higher than 40000 V.

Focusing on an RVD and neglecting the low voltage resistance R_{LV}, which is indeed much lower than the other one, the total HV side resistor could be approximated by

$$R_{HV} = \frac{V_{in}^{\ 2}}{P_{tot}} \qquad (3)$$

where P_{tot} is the maximum power absorbed by the RVD. The maximum absorbed power of the RVD could be chosen about some tens of watts. TABLE I provides the total resistor values for the HV side as a function of the maximum absorbed power. The latter obviously decreases when R_{HV} increases and, on the other hand, the cutoff frequency of the RVD decreases, which is not a desirable effect. It is not easy to quantify here the frequency band variation versus R_{HV}, since cutoff frequency depends also on C_{HV} according to: Cutoff_f (Hz)= $1/R_{HV}.C_{HV}$. Thereupon, considering the values in TABLE I and also according to the available commercial HV resistor values, four 30 MΩ resistors (total of 120 MΩ) are selected for the HV part of the RVD. The total absorbed power in this case will be about 22.5 W. Then, the rated power value for each resistor should be more than 5.6 W, which is compatible with the rated power of the selected commercial resistor (6W) and with the maximum continuous operating voltage of 30 kV.

TABLE I
Values for R_{HV} for different values of absorbed power

Total absorbed power by RVD: P_{tot} (W)	10	15	20	25	30
Total resistor in HV side: R_{HV} (M ohm)	270	180	135	108	90

II.1. Stray capacitances in a VD

It is worth to mention three different stray electric field couplings that give rise to stray capacitances in an RVD as follows:

1- Stray capacitances between the HV elements (here named CHV)

2- Stray capacitances between HV elements and the ground (here named CG)

3- Stray capacitances between the LV elements and also between LV elements and the ground (here named CLV)

These three kind of stray capacitances (CHV, CG, and CLV) will be used to analyze the results of different sensitivity analyses or changes done in the VD configuration.

Neglecting stray capacitance in an RVD, the scale factor $(Z_{HV}+Z_{LV})/Z_{LV}$ will be simply calculated as the ratio of the resistances as (see Fig. 1):

$$SF = \left|1 + \frac{R_{HV}}{R_{LV}}\right| \quad (4)$$

This SF is constant versus frequency (the phase error would be zero). Then if a CHV is added to a pure RVD, Z_{HV} will decrease by increasing the frequency. Then enhancing the CHV in the RVD circuit shifts down the scale factor. It actually acts like a pole of the VD scale factor shown in the following equation:

$$SF = \frac{\left|\overrightarrow{V_{in}}\right|}{\left|\overrightarrow{V_{out}}\right|} = \left|1 + \frac{R_{HV}(\mathrm{j}\omega \mathrm{R}_{LV} C_{LV} + 1)}{R_{LV}}\right| \quad (5)$$

In addition, CHV decreases the phase error of the VD as it reversely acts compared to the scale factor.

Similarly, if a CG is added to a pure RVD (with a flat frequency response), the output voltage will decrease with increasing the frequency. Therefore, the scale factor will be shifted up compared to the pure RVD's one. It actually acts like a zero of VD scale factor as shown in the following equation:

$$SF = \frac{\left|\overrightarrow{V_{in}}\right|}{\left|\overrightarrow{V_{out}}\right|} = \left|1 + \frac{R_{HV}}{R_{LV}(\mathrm{j}\omega \mathrm{R}_{HV} C_{HV} + 1)}\right| \quad (6)$$

The phase error of the VD will also increase.

Correspondingly, if a CLV is added to a pure RVD (with a flat frequency response), the Z_{LV} will decrease with increasing frequency. Consequently, the scale factor will be shifted up compared to the pure RVD scale factor. It acts like a zero of the VD scale factor. It also increases the phase error of the VD.

TABLE II summarizes the effects of different kind of stray capacitances on the scale factor and phase error.

TABLE II
EFFECT OF VARIOUS KIND OF STRAY CAPACITANCES ON FREQUENCY BEHAVIOR

Type of stray capacitances variation / Situation :	SF at higher frequencies:	Phase error at higher frequencies:
If CHV increases:	decreases	increases
If CG increases:	increases	decreases
If CLV increases:	increases	decreases

A simple VD electrical circuit is represented in Fig. 2 as an example for explanation of the relation between CHV and CG. (As TABLE II summarizes) if the CHV (in Fig. 2) is too smaller than the CG, there will be a major drop in SF. In addition, if the CHV is greater than the CG, there will be a lift in SF. Then as explained, designing a new VD with a nearly flat scale factor (and low phase error) is about making the right configuration with right balance between different kind of stray capacitances. This issue is practically shown by using a simple VD electrical circuit (shown in Fig. 2). The frequency behavior of the sample circuit is shown in the Fig. 3. As can be seen the lowest C_G value in the sample circuit does not give the best results and it should be somehow in balance (exactly equal in case of the circuit shown in Fig. 2) with the value of C_{HV}.

In order to predict and calculate the stray capacitances of a VD, a precise and validated model is needed. In this paper the method already proposed in [13] is used to model the new RVD.

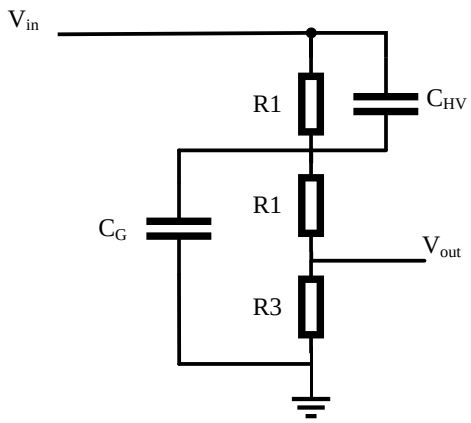


Fig. 2. A sample of an RVD circuit

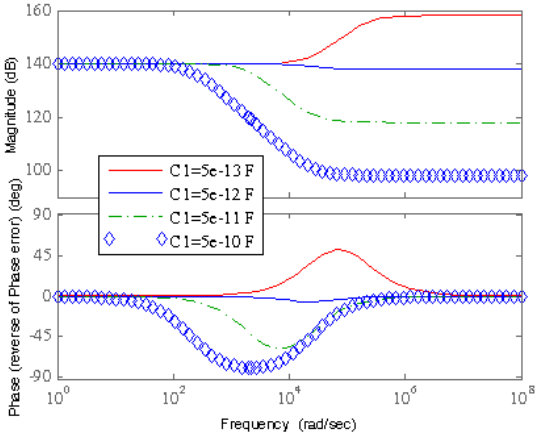


Fig. 3. Bode diagram of the sample VD

II.2. Effect of the introduction of a middle plate

A new arrangement will be analyzed in this section. The best design for an RVD could be obtained in a way that CHVs are somehow independent from two other type of stray capacitances. For example, if the distances between HV resistors and the ground decrease, CG increases which results in an SF overshoot and if those distances increase, the SF decreases with a similar logic. Then, it is better to

make these kind of capacitances less sensitive to geometrical variations. In order to accomplish this target, a new plate between the HV parts and the LV resistors is added. The middle plate is connected to the V_{out} clamp (LV side). The additional plate usually worsen the frequency behavior of the divider but, adding additional capacitors in the LV side, the frequency response can be highly improved.

To verify the effectiveness of the additional plate, the behavior of a simple RVD with and without the LV connected plate is investigated. The configuration of the test VD is shown in Fig. 4. In order to consider the effect of resistor body in stray capacitance calculations and ultimately in VD frequency response behavior, each resistor is divided by two parts (in the FEM model). Each half resistor is connected to the adjacent conductor that connects resistors. The set of each halved resistor plus the adjacent halved resistor and the middle conductor constitutes an electrode.

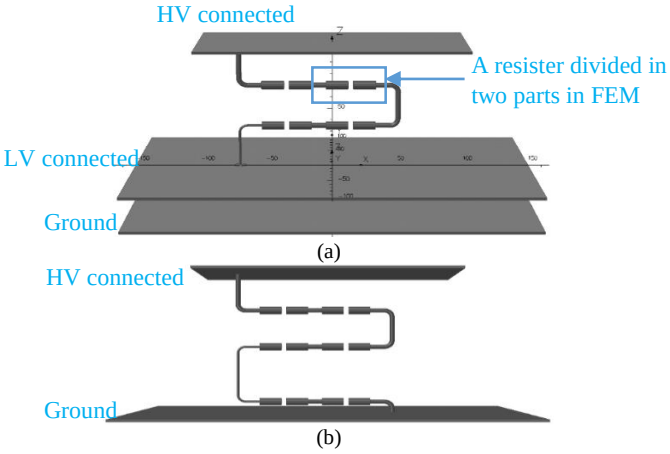
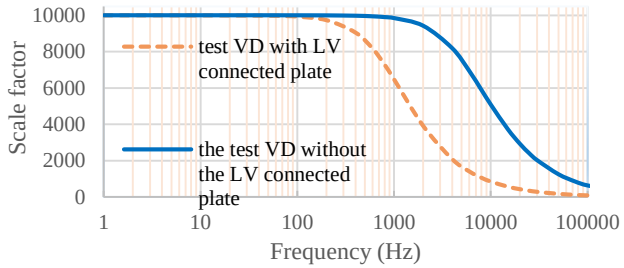


Fig. 4. The geometry of a test VD (a) with middle LV connected plate (a) without middle LV connected plate

The initial result of the test VD is shown in Fig. 5. The initial results proves a better frequency response with higher cut-off frequency in case of the VD without the LV middle plate.



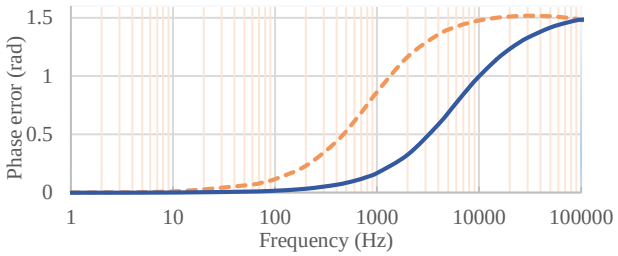


Fig. 5. Result of RVD with and without LV connected plate

Afterwards, an extra capacitance (hereafter named CBT) is added to the output terminals in both cases, that is with and without middle plate. Results of the test VD with added CBT are displayed in Fig. 6. The test VD with LV connected plate (compensated with CBT) shows a better result compared to the test VD without the LV plate (compensated with CBT). The reason is that the VD without the middle plate has overall bigger CG (and less CHV especially between each HV electrode and the LV electrode) -compared to the other case- that cannot be compensated with the CBT. On the other hand, the CGs in the test VD with the middle LV connected plate, are lower and could be compensated by CBT, even if overall CHV is higher. This conclusion is confirmed by comparing the two capacitance matrices of both models.

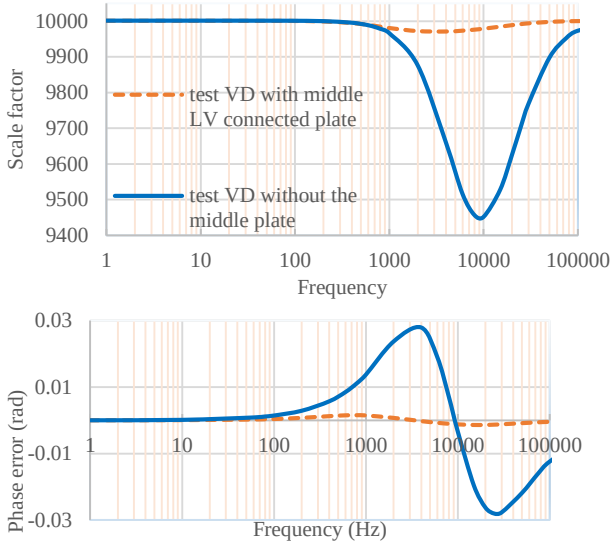


Fig. 6. Results of a compensated RVD with and without LV connected plate

III. MODELING THE HV VD

Due to the high voltage (about 52 kV), the geometrical design should avoid sharp edges from the preliminary design. That is why the HV side and the ground plates with rounded surfaces shown in Fig. 7. The first finite element model (FEM) of the 52 kV VD is presented in Fig. 8. As discussed before, four 30 MΩ, HV resistors (rated voltage 30kV) are vertically placed in the HV section (upper part) of the VD. One 12 kΩ resistor is chosen for the LV part

making the rated scale factor (SF) ratio about 10001. This value may change in the measurement stage due to the discrepancies between the rated value of the resistors and their measured (actual) values. The HV resistors are placed vertically in order to decrease the stray capacitances due to the coupling between HV electrodes and the ground plate.

Furthermore, in order to avoid electric field hot-spot and corona effect, copper tube with 2mm diameter (instead of a simple wire) is chosen as conductors connecting resistors to each other and also to the plates.

(a) (b)

Fig. 7. The HV and ground plates with round edges (a) top (outside) view (b) bottom (inside) view

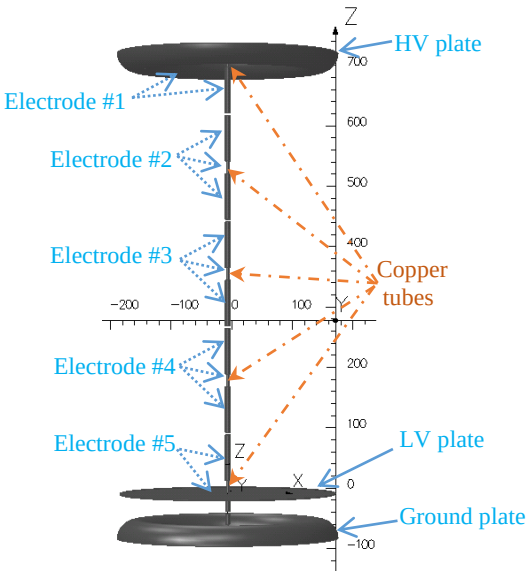


Fig. 8. Geometry of the vertical 52 kV RVD (electrodes modeled in FEM are numbered in the picture. The #1 is the HV plate and the #5 is the LV plate.)

III.1. Considering of grounded floor (importance of grounded floor modeling)

Any object with floating potential or a certain voltage near the VD can introduce stray capacitances between its surface and each electrode of the VD, both in the HV and LV sections. The main object near to the VD, in every environments, is definitely the grounded floor. In order to model the floor, a surface below the grounded plate of the vertical VD with assigned zero potential is added to the FEM model.

In order to demonstrate the effect of the grounded floor, two different models without and with the plane mimicking the grounded floor are simulated and are shown in in Fig. 9 and Fig. 10, respectively. The insulation pillars and the insulation supporting the HV resistors are also modeled as they can change the electric field course and consequently the stray capacitances. The relative permittivity of the pillars and resistor support is assumed to be equal to 2.9.

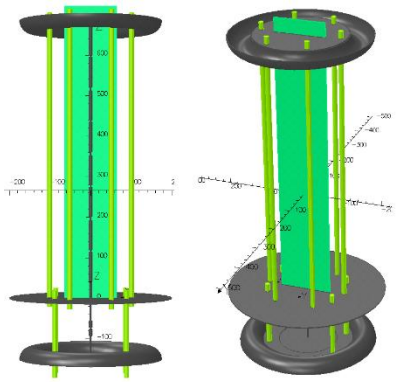


Fig. 9. The model without the grounded floor

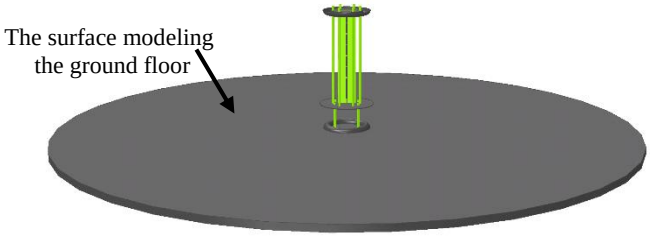


Fig. 10. The model considering the grounded floor

IV. MEASUREMENT SET UP

The set up used for measurement of the frequency behavior of the VD is shown in the Fig. 11 [13] and Fig. 12. The voltage produced by voltage calibrator is applied to the HV plate at top of the VD. This voltage is measured by the first digitizer -Agilent 3458. The output of the VD is then measured by the second digitizer -Agilent 345. The Voltage calibrator, and two digitizers are synchronized using a signal generator - Fluke397- in order to correctly measure the phase difference between two HV and LV signals.

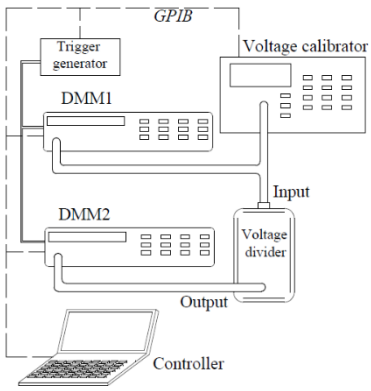


Fig. 11. the measurement set-up[13]

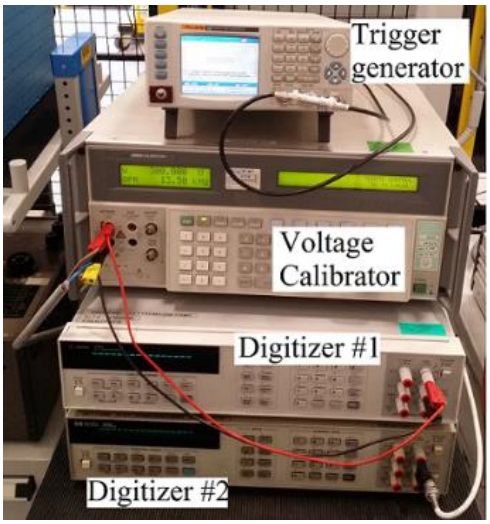


Fig. 12. The measurement setup (excluding the VD)

The realized vertical 52 kV RVD is also represented in Fig. 13.

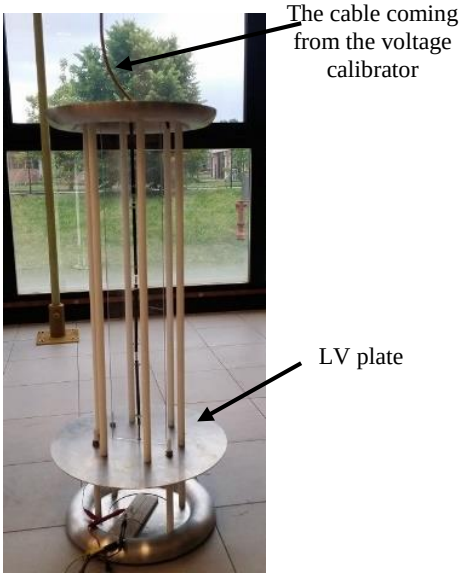


Fig. 13. Vertical 52 kV RVD

Preliminary results of the 52 kV RVD are shown in Fig. 14. As can be seen modeling the floor has a great effect on the simulation results of the VD. As explained before, the values of CG are underestimated when the ground floor is not considered in the simulation. That is why there is a decrease of cut-off frequency in both scale factor and phase error of the simulation when not considering the ground floor surface.

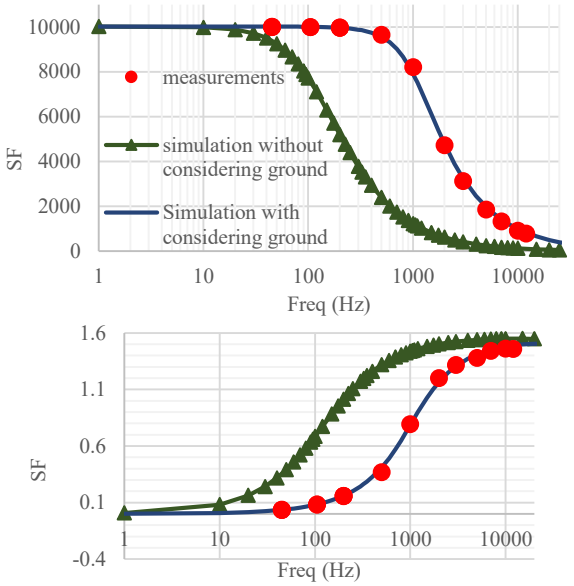


Fig. 14. Initial Results of 53kV RVD

The simulation results of the vertical RVD with the ground plane and compensated with a capacitor in the output -CBT- is presented in Fig. 15.

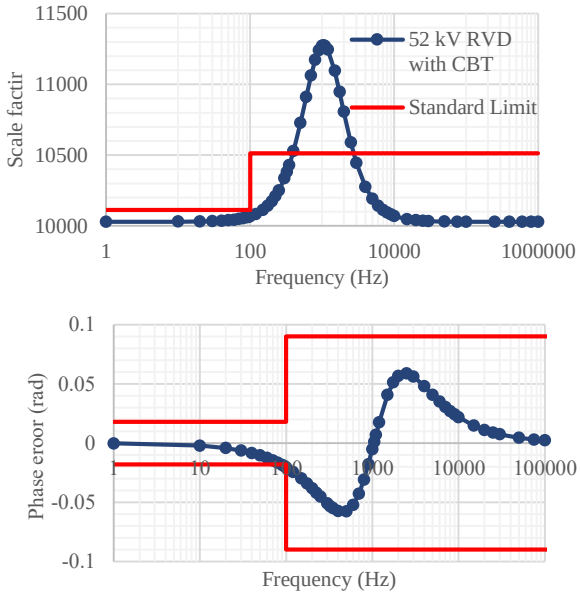


Fig. 15. The result of the vertical RVD with LV compensation capacitor (CBT)

The result of vertical VD shown in Fig. 15 has a max SF deviation of 12% from the rated value and also a maximum phase error of about 60 mrad. These results cannot meet the requirement of a standard VD. The reason is clearly due to the excess of coupling between the ground and the HV section of RVD (increased CGs).

In order to decrease the CGs, the electric field coupling between the HV electrodes and the ground should be weakened. To this reason a shield is added to the RVD being connected to the LV plate as shown in Fig. 16. The height of the shield is chosen equal to 150 mm since each HV resistor length is about 150mm and the copper jointing the lowest HV resistor to the adjacent one has a 190mm distance from the LV plate (displayed in Fig. 16). Therefore, the height of 150 mm is chosen in order to avoid the presence of the high voltage near to the edge of the LV shield.

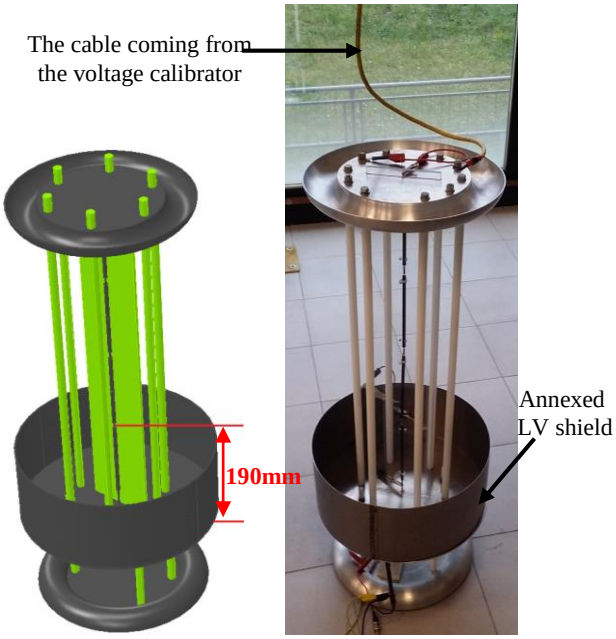
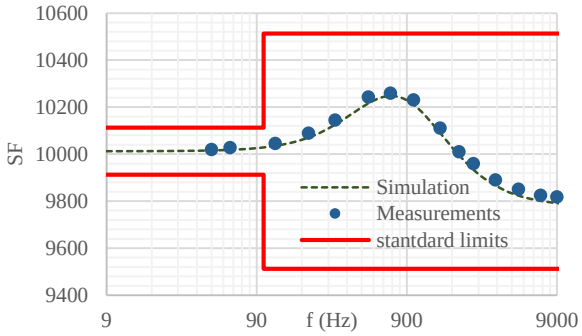


Fig. 16. The simulation and realized 52 kV vertical RVD with LV shield

The result of the 52 kV RVD with LV shield and compensated by a capacitor in the LV side is shown in Fig. 17.



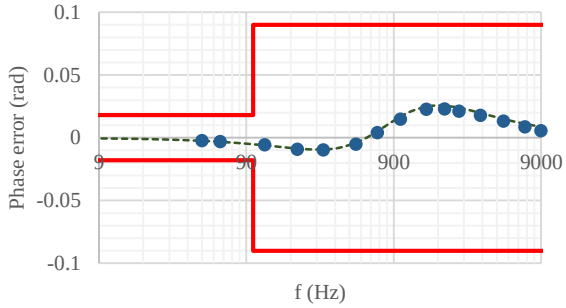


Fig. 17. Results of 52 kV RVD with LV shield and compensated by a capacitor
Fig. 18

V. CONCLUSION

Acknowledgements

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