

Development of a PJVS System for Quantum-Based Sampled Power Measurements

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Abstract

The paper deals with recent progresses at INRiM towards the development and characterization of a programmable Josephson voltage standard (PJVS) operating in a small liquid helium dewar as well as with its integration for the realization of a practical quantum sampling electrical power standard. The PJVS is based on a 1 V superconductor-normal metal-superconductor (SNS) binary-divided array of 8192 Josephson junctions. To ensure proper operating conditions of the PJVS chip, a custom short cryoprobe was designed, built and successfully tested. The overall system is being developed in the framework of EMPIR project 19RPT01-QuantumPower. The goal is to establish a new quantum power standard (QPS) based on a single Josephson voltage standard for sampled power measurements and to gain confidence in running PJVS for precise calibration of digital sampling multimeters and arbitrary waveform digitizers used in the ac-voltage and power metrology community.

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1. Introduction

In the era of clean energy transition, the electrical power system is witnessing a rapid growth of renewable energy sources with unprecedented levels of integration and rapid decarbonisation of the electricity supply chain. For stable operation of smart grids, precise and traceable electrical power measurements are required to guarantee stable supply, prevent blackouts, identify the origin and causes of the disturbances, and ensure a fair electricity market. National metrological institutes (NMIs) are working closely with network operators to face the electricity system and grid paradigm shift in response to the EU energy transition and clean energy target.

Presently, in most NMIs, the primary electrical power has traceability to the volt and ampere employing a long and time-consuming calibration chain, which involves the use of thermal converters, voltage and current transducers and high-precision digitizers. Most recent implementations show that this calibration chain enables sampling-based power measurements with a relative uncertainty ranging from $1\ \mu\text{W}/\text{VA}$ to $10\ \mu\text{W}/\text{VA}$ (coverage factor $k = 1$) at power-line frequency and at any power factor [1–3]. Moreover, only a few experimental setups have been proposed among the NMIs, aimed at integrating the ac-quantum voltage standards into sampling power standards [4–6] to provide power measurements with less uncertainty.

In particular, in the framework of the EMPIR project 19RPT01 - Quan-

tumPower [7], a strong collaboration is taking place between several NMIs to deliver the necessary infrastructure for validated quantum-referenced power measurements and its availability to industry. The initiative brings together the experience gained during the last two decades by the involved NMIs in the field of quantum voltage and electrical power. The project aims to design and build an open-access quantum sampling electrical power standard, which will lead to increased confidence in power measurements used for calibration and validation of standard wattmeters, static energy meters, phantom power sources, power analyzers and new emerging equipment for monitoring and identification of electricity-grid stability parameters, where confidence and traceability are crucial. The new quantum power standard will benefit from the use of a programmable Josephson voltage standard (PJVS), which plays a crucial role in the redefinition of the volt unit in the new quantum SI. The integration of PJVS enables real-time calibration of gain and linearity of high-precision analogue-to-digital converters (ADCS) and digitizing multimeters (DMMs) used in primary sampling power standards. The target uncertainty is less than $2\ \mu\text{W}/\text{VA}$ for the contribution of digitizers in power measurements. Figure 1 shows the conceptual block diagrams comparing the conventional power standard and the QPS system developed in the framework of this project.

The research activity carried out at the Istituto Nazionale di Ricerca Metrologica (INRiM) in the framework of the QuantumPower project foresees the integration of two main key components into its sampling power standard based on wideband analog-to-digital converters (ADCs) [3]: i) an ac-programmable Josephson voltage standard, and ii) a synchronous coaxial

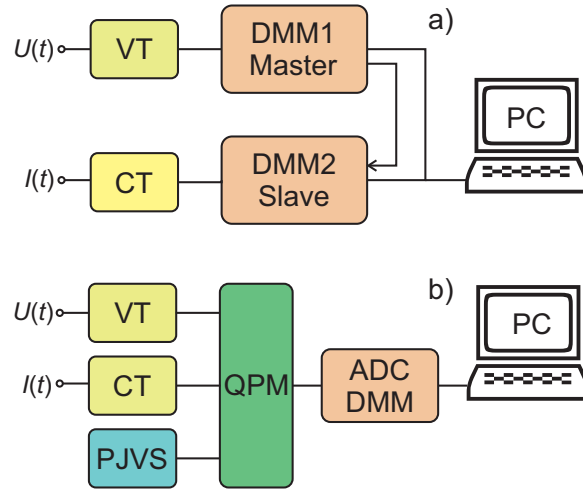


Figure 1: Conceptual block diagrams. a) conventional single-phase sampling power standards with voltage and current transducers; b) sampling quantum power standard with transducers developed in the framework of the EMPIR project 19RPT01-QuantumPower.

QP-multiplexer. This will allow to shorten the traceability chain employed for the calibration of the sampling power standard as much as possible by ensuring a direct link of sampled power measurements in the new quantum SI, and therefore a reduction in the measurement uncertainty.

The present paper reports progress towards the development and characterization of a PJVS, its integration into the INRiM sampling power standard for single-phase power measurements, and first measurements for the validation of the whole setup, namely the quantum power standard (QPS). As the development of such a PJVS-based system at INRiM is new, it was necessary to carefully design and characterize almost all its constituents. Our intent was to develop a compact PJVS-based system, cooled down in a small liquid helium (LHe) dewar, to be easily transported. A custom short cryoprobe was built to ensure suitable operating conditions of the PJVS array. The

maximum output voltage of the PJVS array was chosen to be close to the output voltage level of voltage and current transducers in use at the INRiM primary power and energy laboratory, whose rms voltage never exceeds 800 mV applying nominal quantities to the voltage and current transducers inputs.

In general, the adoption of PJVS into the sampling power standard for the realization of a practical QPS has been accompanied by the identification of a suitable multiplexing strategy [8] and the development of new synchronized QP-multiplexer by the project partners [9]. To ensure proper working of the QPS, an open source software, novel measurement methods and algorithms for data processing have been developed [10] and tested.

A first validation strategy of the QPS implementation, without using voltage and current transducers, is purposed and presented in the present paper. Its aim is to generate two low-voltage sinusoidal waveforms, U_1 and U_2 , that QPS will measure under normal operating conditions. The measurement results will be compared against those obtained with the INRiM digital sampling power standard (DSPS)¹ [3]. For the generation of the two low-voltage sinusoidal waveforms, a two-stage inductive voltage divider (IVD) and an AC calibrator have been used. The IVD is used as voltage ration transfer standard, since it enables the generation of two voltages whose ratio, $R = \frac{U_2}{U_1}$, is

¹The DSPS was developed in the framework of EMPIR project TracePQM (15RPT04) [11]. Its modular structure enables low-frequency power measurements, using synchronized digital multimeters (DMMs), or high-frequency power measurements, using wide-band analog-to-digital converters (ADCs)). It was validated in the framework of INRiM participation in the international key comparison EURAMET.EM-K5.2018 [12].

close to the IVD nominal ratio and almost independent of temperature and humidity variations. Although this method does not reveal possible systematic errors in the measurement of the absolute rms-value of the voltages $U_{1,2}$, it has been taken into account due to its simple implementation and the fact that the IVD can be easily transported between the two measurement setups under comparison.

2. PJVS system details

It is well known that binary-divided Josephson arrays provide quantized voltages according to fundamental Josephson equation for quantum voltage metrology,

$$U(t) = nM(t)\frac{h}{2e}f, \quad (1)$$

where n denotes the order of the Shapiro step, M represents the number of Josephson junctions in the “active” state, h and e are the Planck constant and elementary charge, respectively, and f is the frequency of the microwave field radiating the Josephson junctions. For proper operation of a PJVS device, two additional conditions must be fulfilled: a) cooling down the array to cryogenic temperatures, e.g. around 4.2 K, and b) rapidly biasing different sub-arrays containing different number of junctions.

At present, both low-frequency current bias and microwave radiation are provided by conventional electronics operating at room temperature, so the connection between the cryogenic environment and room-temperature electronics is performed by using a purposely-designed cryoprobe. In the following we report details about the main equipment used for running the PJVS

system.

2.1. Consideration on the LHe dewar

The PJVS system will be used for both calibration and research purposes, therefore compactness and transportability are the two requirements which need to be fulfilled. To meet this need, a small LHe dewar designed and manufactured by Precision Cryogenic Systems, Inc. has been used in the proposed experimental setup. The dewar was dimensioned to contain 30 l of LHe and its overall height is about 67 cm. Its reduced height makes it possible to shorten the length of the cables and therefore minimize the systematic errors due to the voltage leads in AC-Josephson standards.

The internal vessel is made of aluminum and the lower inner part is similar to a cylindrical glass with diameter of about 7.73 cm and about 20.3 cm high. This is the useful part dedicated to the experiment and it is wrapped out with a cylindrical AD-MU-80 magnetic shield. First experiments showed that the dewar evaporation rate is about 6-7 l/day, comparable with conventional dewars and sufficient for calibration purposes. Figure 2 reports the dewar equipment and the top part of the custom home-made cryoprobe.

2.2. Custom short cryoprobe design

Figure 3 reports a picture of the custom short LHe-cryoprobe designed to properly host the 1 V PJVS array. Its main support is a low conductivity stainless steel tube with diameter of about 28 mm and length of 70 cm. Internally, an oversized circular waveguide with diameter of about 14 mm and length of 80 cm has been installed. The key parameters of the oversized circular waveguide are: low-microwave loss (attenuation 1 dB/m to

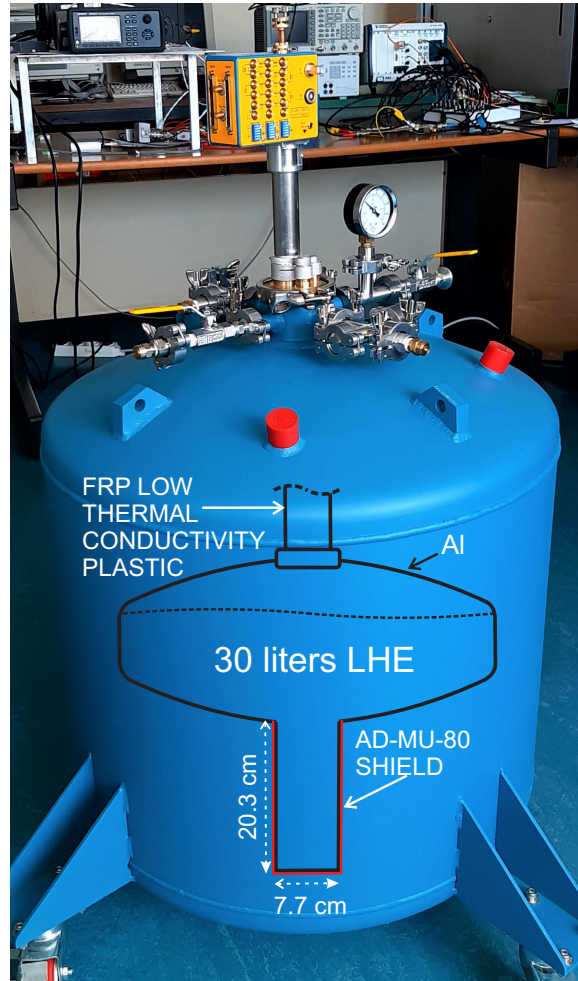


Figure 2: Photograph of the dewar and its schematic of the internal structure with the short cryoprobe inserted and the equipment to ensure safety operation during its use.

3 dB/m at 70 GHz to 75 GHz); made with low thermal conductivity material (Cu–Ni–Zn alloy and wall thickness 0.5 mm); temperature operating range from 1 K to 400 K; frequency range from 60 GHz to 90 GHz. The waveguide is plugged into the chip carrier mount flange (see Fig. 3c for details) by a thin polyethylene sheet inserted between the WR-12 flanges. Since the cryoprobe is significantly shorter than cryoprobes for common higher-capacity dewars, particular attention has been paid to both its design and the choice of the materials employed for its construction for minimizing the thermal load and hence to prevent excessive LHe consumption. The outermost stainless steel hollow tube of the cryoprobe acts itself as an RF shielding and, at the lower end, a 1.5 mm thick magnetic shield made of CRYOPERM 10 is installed. In fact, in the present setup, a total of two magnetic shields (one at the end of the designed cryoprobe and the other at the lower end of the inner vessel of the dewar) are used. This ensures a complete shielding of the PJVS avoiding as much as possible the electromagnetic interferences, as well as the occurrence of magnetic flux trapping within the Josephson junctions. Additional key features of the cryoprobe include:

- top sealed cryoprobe to allow sample cooling using a conventional two-step cooling process leaving the sample inserted in the dewar, i.e. pre-cooling with liquid nitrogen (LN) and then cooling with liquid Helium (LHe) after removing all the LN;
- helium gas escapes from the dewar through a plumbing system of ball valve and pressure release valve located on the top of the LHe dewar.

The pressure inside the dewar is kept constant by using either the pressure-

released valve or a flow impedance realized with a small diameter hose using gas hose couplings (quick connectors).

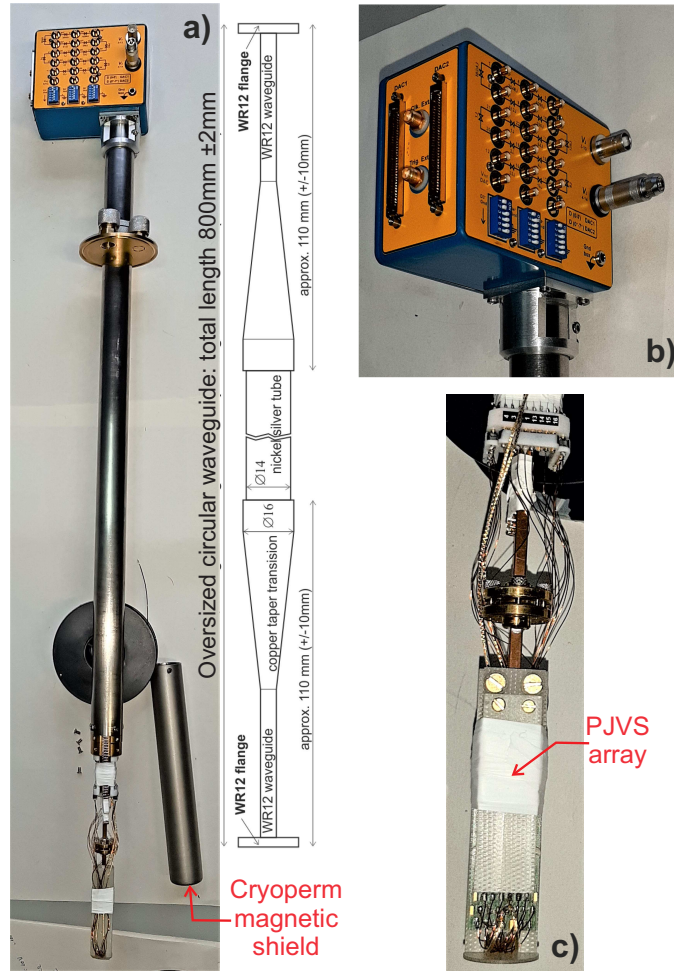


Figure 3: Home-made short cryoprobe designed for hosting the PJVS chip: a) photograph of the short cryoprobe and the Cryoperm magnetic shield; the PJVS chip carrier is mounted in its center; b) head box with connectors; c) chip carrier with installed PJVS array - not visible because placed between two plastic cover plates - plugged with WR-12 flange to the oversized waveguide; the WR-12 waveguide is terminated with a small horizontal aperture where the on-chip finline antenna is inserted into.

2.3. SNS programmable Josephson array

The PJVS chip is a binary-divided array containing 8192 Josephson junctions fabricated by Supracon. The N-material is amorphous $\text{Nb}_x\text{Si}_{1-x}$ alloy near the metal-insulator transitions tuned for operation at about 70 GHz. The array presents quite similar features to those fabricated in the framework of NIST-PTB collaboration [13]. Its main parameters can be summarized as follows:

- $V_C = I_C \cdot R_N \approx 160 \mu\text{V}$, with V_C the characteristic voltage, I_C the critical current and R_N the normal resistance, which corresponds to a characteristic frequency of about $f_C = 77 \text{ GHz}$;
- Critical current $I_C \approx 4.9 \text{ mA}$ at 4.2 K; 0th order Shapiro step width $\leq 4.3 \text{ mA}$; 1st order Shapiro steps width and center for all-subsections $\leq 3 \text{ mA}$ and $\approx 5 \text{ mA}$, respectively.

The array is segmented in 14 subsections, each of which can be independently current-driven to a given quantum step, usually zero and first order. Starting from the low-voltage terminal, the number of junctions in the sub-arrays follows the binary sequence of [32, 16, 8, 4, 2, 1, 1, 64, 128, 256, 512, 1024, 2048, 4096]. Two separate single-junction sub-arrays are necessary to perform a highly accurate quantization test and to determine the PJVS quantum operating margins.

2.4. Wiring and connectors

Wiring of the PJVS chip at room temperature electronics requires some precautions to avoid as much as possible phenomena due to flux trapping and

electromagnetic interference. The cryoprobe has been equipped with suitable cryogenic wires as follows:

- 12 twisted-pairs for a total of 24 wires of beryllium-copper (BeCu) wires of $100\ \mu\text{m}$ diameter and $10\ \Omega/\text{m}$ resistance (independent of temperature) are used for current biasing the PJVS subsections. Only 14 out of the 24 wires are actually used. Relying on theoretical assumptions, the thermal load of such a twisted-pairs cable compared to conventional twisted-pairs Cu cable leads to a LHe vaporization rate reduction by a factor of 10.
- The PJVS device is suitably installed on a chip-carrier and bonded on finished gold PCB pads with aluminum wires. 14 pads are used to provide connection of the single subsections to the biasing electronics. High (V_H) and low (V_L) voltage Josephson array terminals are bonded on two separate PCB pads. Two ultra-miniature coaxial cryogenic cables with inner conductor of stranded copper isolated in Teflon from its outer conductor, made of braided gold-plated copper, were used to transfer the Josephson quantized voltage from 4.2 K to room temperature. In the first configuration, each coaxial cable has been directly soldered to the PCB pads dedicated to the Josephson voltage. However, it is possible to redefine the connections by using the inner conductors of each coaxial cable to bring out the Josephson voltage to room temperature, which seems the most promising configuration to ensure greater immunity from EMI interferences and phenomena related to the generation of thermal electromotive forces between the wires and the PCB pads.

- The cryoprobe head is fixed to the main stainless steel tube with a removable sealing mechanism and, in order to avoid the escape of cold helium vapors, its upper side is sealed with a bicomponent epoxy resin. It is equipped with both 16 coaxial SMB connectors and two 68 pin I/O connectors for quick connection to the biasing electronics. A triaxial LEMO connector was used for the Josephson voltage output. Its fixing ensures a good electrical and thermal decoupling from the cryoprobe head, thus avoiding unwanted thermal gradients, which could give rise to thermal electromotive forces.

3. Experimental setup for PJVS array characterization

A photograph of the overall experimental setup employed for testing and using of the PJVS array is shown in Fig. 4.

It is composed as follows:

3.1. *I-V fast monitoring setup*

The current-voltage ($I - V$) characteristics of the single sections of the PJVS array, with and without microwave radiation, have been recorded using a fast-tracking fully digital system [14]. High-speed digitizers or high-precision digital multimeters, e.g, DMM-3458A, can be used for the recording of voltage and current signals.

3.2. *RF/Microwave generation system*

During the first experiment, the array was irradiated using alternatively two Gunn oscillators, capable of covering a frequency range from 70 GHz to about 73 GHz. The RF power at the input flange of the circular waveguide

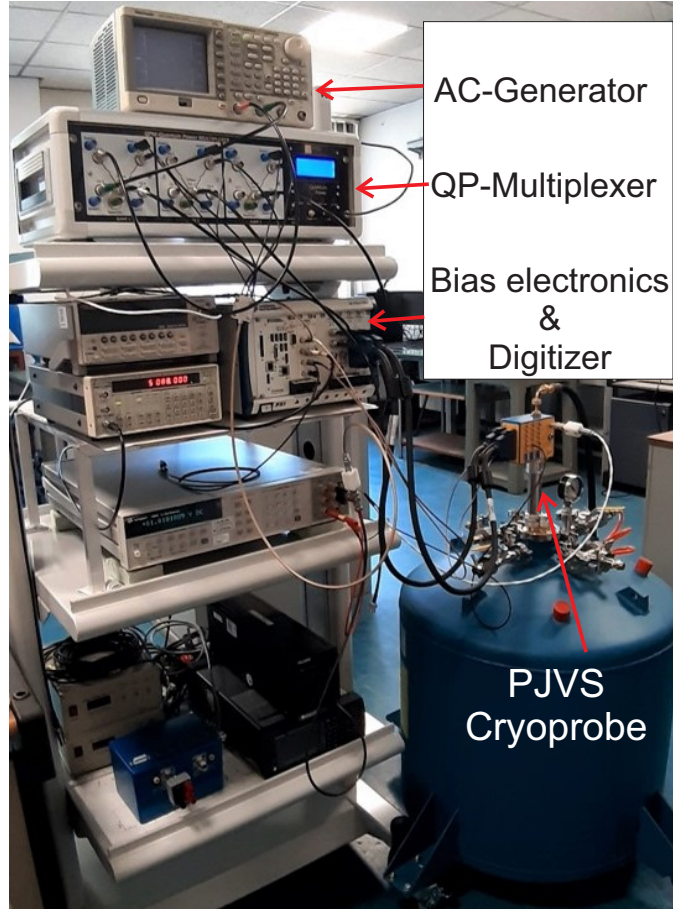


Figure 4: Photograph of the experimental setup employed for: i) PJVS array characterization; ii) quantum power standard (QPS) which integrates the PJVS system, the synchronous QP-multiplexer and high-precision NI PXI-5922 digitizer. The PJVS bias electronics, clock and trigger sources and PXI-5922 are integrated into a PXIe chassis with embedded PC controller. The AC-generator is used for testing purpose.

was about 30 mW, which ensures almost equal width of zero and first order Shapiro steps.

A second RF generation chain has been set up to conduct the various test, which allows to accurately know the microwave frequency. The RF source selected, to get useful quantized voltage steps, is a fully-synthesized signal generator equipped with a signal generator extender². Additionally, a RF power amplifier having a 4 GHz bandwidth centered at 73 GHz and -3 dB gain attenuation to its bandwidth has been inserted between the output of the signal generator extender and the WR-12 input flange of the cryoprobe circular waveguide. The overall RF generation system enables to deliver enough power to ensure proper array operating conditions from 71 GHz to 75 GHz and it is phase-locked to the 10 MHz reference clock traceable to the INRiM atomic frequency standard.

4. PJVS measurement results and discussion

First characterization of the system and PJVS array concerned the determination of $I - V$ characteristics with and without RF radiation. The $I - V$ characteristic of the full array without RF radiation is reported in Fig. 5, where it is clearly observed that I_C at 4.2 K is slightly less than 5 mA.

²The RF signal generator is an Agilent E8257D capable of generating signals up to 20 GHz. Its frequency has been extended using an OML S15MS-AG millimeter-wave source module for operation in the range 50 GHz to 75 GHz.

Brand names are used for identification purpose. Such identification does not imply recommendation or endorsement by INRiM, nor does it imply that the equipment identified is necessarily the best available for the purpose.

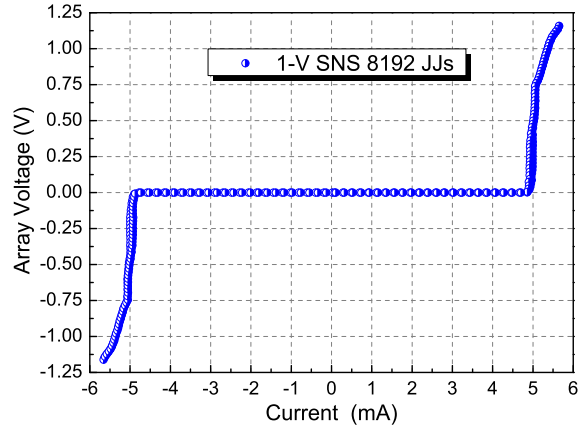


Figure 5: $I - V$ characteristic for the determination of 1 V PJVS array critical current in LHe.

The second series of tests was focused on the determination of current-width and flatness of the quantized voltages across each PJVS sub-array by irradiating the array from 70 GHz to 73 GHz. Fig. 6 reports only the results obtained at 72 GHz.

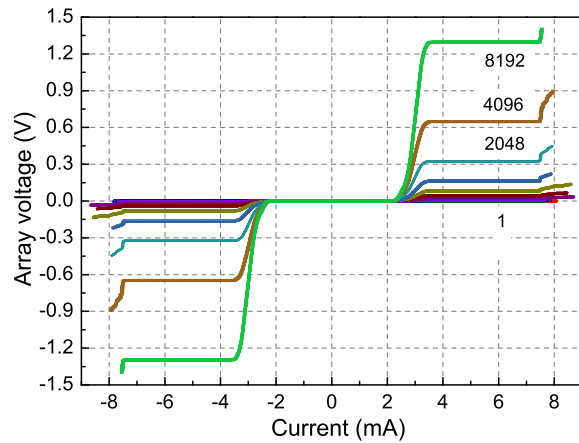


Figure 6: $I - V$ characteristic of PJVS subsections under constant RF radiation at 72 GHz.

As shown in Fig. 6, quantized voltage corresponding to $n = -1, 0, +1$

Shapiro steps are clearly visible for all the PJVS subsections. The RF power has been trimmed to ensure almost similar operational current margins for each section. The operational current margins for Shapiro step orders -1 , 0 and 1 result to be within 3 mA, which are large enough to simplify proper operations of the array for experiments related to the synthesis of staircase sinusoidal waveforms.

Fig. 7 reports a high-resolution plot as a demonstration of the flatness of $n = +1$ Shapiro steps.

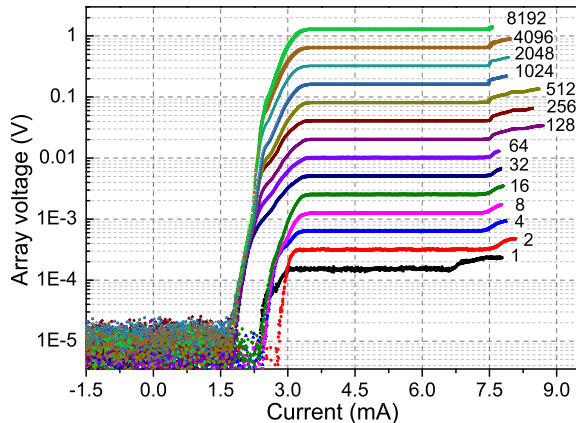


Figure 7: $I - V$ characteristic of PJVS subsections at 72 GHz; logarithmic voltage scale.

The excess noise observed is due to the fast $I - V$ tracking setup. During the first experiment run, we observed a significant thermal EMF (about $50 \mu\text{V}$) superimposed to the Josephson voltage output wired with the cryogenic coaxial cable. Instead, the thermal offset across the BeCu twisted-pairs, used for current biasing of PJVS subsections, was lower than $1 \mu\text{V}$.

Further tests have been carried out with a short piece of the same coaxial cable, short-circuited at one end, mounting the same end on the 4 K stage of a pulse-tube cryocooler. The experiment confirmed that large thermal EMF

appears, probably due to the different material composition and Seebeck coefficient between center conductor and shield of the coaxial cable.

It is worth mentioning that, after further improvements of the cryoprobe wiring, using only the inner conductors of both miniaturized coaxial cables to bring out the Josephson voltage to room temperature, the residual thermal EMF measured across the PJVS output is reduced to a value less than 100 nV.

4.1. Step flatness quantization test

In order to demonstrate that the programmable Josephson voltage standard is working properly, we performed the aforementioned quantization test irradiating the array. To this aim, half array (4096 junctions) is current-biased to the $n = +1$ Shapiro step, whereas the second half is biased to the $n = -1$ step. The PJVS output voltage is then exactly zero for bias currents within the quantum margins, and is measured with a digital nanovoltmeter.

Several bias sequences were generated and loaded to the PJVS bias electronics. Each sequence corresponds to a well-defined current bias value chosen in according to the operating margins observed for all subsections as shown in Fig. 7. The bias current ranges from 4.4 mA to 6.4 mA and the array output is recorded with a digital nanovoltmeter.

The results are reported in Fig.8. The nanovoltmeter readings at the specific bias current have been corrected by the value of the thermal EMF.

4.2. Synthesis of quantum-based staircase sinusoidal waveforms

A second round of tests was conducted in order to validate the PJVS setup as a whole, for the direct synthesis of quantum-based staircase sinusoidal waveforms. Fig. 9 shows four different sine waves at 53 Hz composed of 10

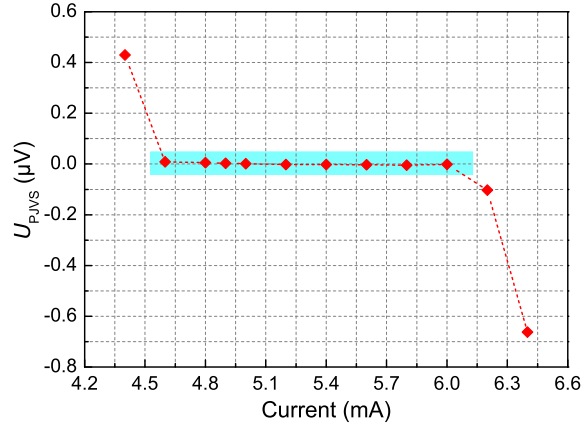


Figure 8: Step flatness quantization test of the 1 V PJVS at 72 GHz.

steps, which differ mainly by the bias current used to switch on/off the PJVS sections. The RF frequency was set to 72 GHz.

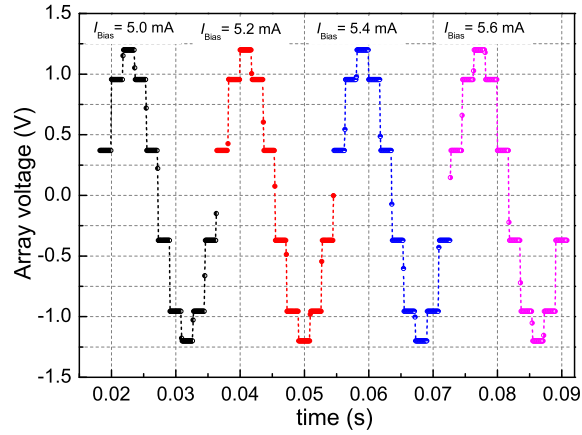


Figure 9: Staircase sinusoidal waveforms synthesized with different bias currents.

By comparing the various voltage steps sampled by means of a high precision sampling digital multimeters, e.g. Keysight 3458A, at 10 kS/s and aperture time 90 μ s, we found that the relative voltage difference between the quantized voltage steps at different biasing currents is lower than 1 μ V/V.

4.3. DC and AC validation of PJVS

A series of experiments have been carried out to validate the PJVS system in both DC and AC regimes. For the DC validation, a simple experimental setup and a triangular comparison strategy have been adopted for direct comparison of the 1V PJVS against two Zener-based voltage standards (Fluke 732B), previously calibrated against the Italian maintained DC voltage standard at 1.018 V [15]. The self-consistency of the method has been verified by computing the residual difference of the triangular closure, which is about 0.2 μ V and sufficient for use of PJVS in power measurements.

With regards to the AC validation, Fig. 10 shows the results of an equivalent quantization test using 16 steps staircase-approximated sine waves synthesized at different bias-current setpoints and at constant microwave frequency and RF power. A high precision digital multimeter is used for sampling the synthesized stepwise waveforms. Both the update frequency of the PJVS bias source and the sampling frequency of the DMM are synchronized to the 10 MHz national reference clock, making it possible coherent sampling of staircase sinusoidal waveforms. Further experimental details are reported in [16].

The obtained results confirm that the PJVS system is working in both DC and AC and is ready to be integrated into the INRiM sampling power standard for the realization of the quantum power standard.

5. Adaption of PJVS for sampled power measurements

For the realization of the QPS, the PJVS alone is not sufficient and must be integrated with other equipment. In fact, the QPS setup agreed within

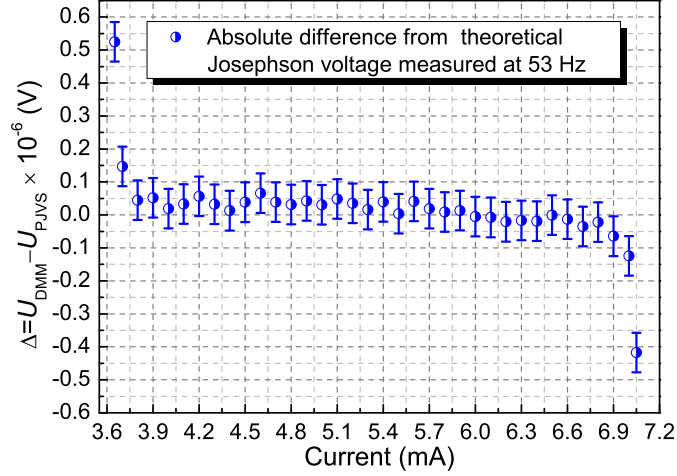


Figure 10: AC quantization test with staircase sinusoidal waveforms (53 Hz, 16 steps) sampled with a high precision DMM. Blue dots represent the absolute difference, $\Delta = U_{\text{DMM}} - U_{\text{PJVS}}$, where U_{DMM} is the rms value of the PJVS sine waves at different bias currents, computed after deleting data sampled during the transients as, $U_{\text{rms}}^2 = \frac{1}{m} \sum_{i=1}^m U_i^2$ with m number of remaining points within a period, whereas U_{PJVS} is the rms value of the theoretical Josephson voltage. The error bars represent the Type A uncertainty. The DMM sampler was set to 1 V full-scale, sampling frequency 5.088 kHz, aperture time 150 μs and 10s total acquisition time.

the project aims to overcome on the one hand the cost and excessive development effort by individual partners and, on the other hand, to introduce new insights into the use of PJVS standards in the field of electric power and its derivatives, such as power quality and synchronized measurements of voltage and current in smart grids.

The QPS is a complex experimental setup and its main constituents can be summarized as follows:

- PJVS for direct synthesis of quantum-based staircase sinusoidal waveforms up to the kHz range and amplitude up to 2 Vpp.

- Synchronized digital multimeters (DMMs) or high precision analog-to-digital converters (ADCs), e.g., HP/Agilent/Keysight 3458A or NI PXI-5922), for single phase or three-phase power measurements. It is worth mentioning that up to six synchronized waveform samplers are required for conventional three-phase power measurements, which have never been performed with electrical quantum standards so far. The project is paving the way to carry out quantum based three-phase power measurements by using a reduced number of waveform samplers, only one PJVS standard and the synchronized QP-multiplexer specially designed and built by project partners.
- Synchronized QP-multiplexer for serializing in a single stream the quantum-based staircase sine-wave and the sinusoidal waveforms coming from voltage and current transducers [9]. The full version of the QP-multiplexer contains three slave boards in the configuration 4-to-1, i.e., each slave board has four independent guarded coaxial inputs and one guarded coaxial output. Several QP-multiplexers have been developed and characterized by project partners and are now part of the QPS. Insights about the multiplexing strategies to carry out quantum-based single-phase or multi-phase power measurements are reported in [8].
- Trigger & clock distribution system, frequency-locked to the 10 MHz reference signal distributed starting from the INRiM atomic clock.
- Open source software, namely QPS software, developed in the scope of project [10, 17].

The adaptation of the AC-PJVS into the QPS for sampled power mea-

measurements has been successfully completed and minor issues regarding the optimization of experimental strategies for robust and reliable triggering of the main QPS constituents are still in testing phase.

5.1. QPS implementation and preliminary validation

The first version of the QPS setup, suitable for quantum-based single phase electrical power measurements, has been implemented and tests for its validation are being carried out. The various QPS versions developed by the project consortium differ slightly according to the PJVS configuration owned by each partner. Fig. 11 shows the experimental setup employed for the preliminary validation of the QPS implementation at INRiM.

A possible validation strategy of the QPS, without considering the voltage and current transducers, consists in using a two-stage inductive voltage divider. The ratio of an IVD is defined as follows: $R = \frac{N_2}{N_1} = \frac{U_2}{U_1}$, where N_1 is total number of turns, N_2 number of turns at the tap, U_1 the IVD input signal provided by an AC calibrator, U_2 the output voltage at different IVD taps.

The IVD is a two-stage inductive voltage divider having twenty output-taps designed for linearity calibration in AC of high precision digital multi-meters, employed in the primary power standard [3]. It has been recently redesigned and its ratio and phase errors are within 1×10^{-6} and $6 \mu\text{rad}$ for voltages from 1 V to 10 V and frequencies from 40 Hz to 400 Hz.

Amplitude and relative phase shift of U_1 and U_2 voltages are measured using both QPS and DSPS setups. Ratio and phase errors at each IVD tap are computed starting from the measurement data and the results are reported in Fig. 12 and Fig. 13. As shown in Figs. 12 and 13, the deviation of

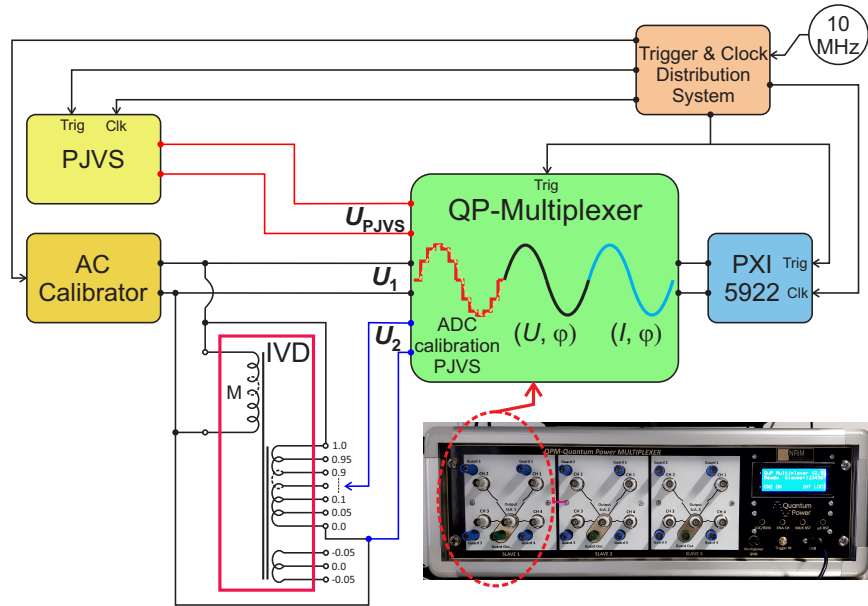


Figure 11: Simplified schematic of the methodology developed for the comparison of the QPS configured for single-phase power measurements. The trigger & clock distribution system employs: i) NI PXIe-5451 dual-channel arbitrary waveform generator for synthesis of trigger and clock signals useful for the PJVS current bias source; ii) Agilent 33120A for the generation of the trigger signal for QP-multiplexer and PXI-5922; iii) Synthesized clock generator SR-CG635, with random jitter less than 1 ps rms, for 10 MHz reference clock generation linked to the INRiM atomic frequency standard.

the IVD ratio and phase errors measured with the QPS and DSPS are within 10 ppm and 12 μ rad. All the measurements were carried out at 50 Hz and at nominal voltage of 0.8 V. At first sight, the deviation of the measurement results are to be attributed to the QPS setup. In particular, it is observed that amplitude and phase measurements carried out with the QPS system are affected by the synchronization lack of the AC voltage calibrator. To address this issue, a different synchronization approach is being developed,

which consists in connecting the *phase-lock-in* input of the AC calibrator to the trigger and clock distribution system, as shown in Fig. 11, and the results will be presented in future publications. Additional noise sources are still being investigated and research is underway to mitigate possible errors caused by interference and ground loops between the QPS constituents.

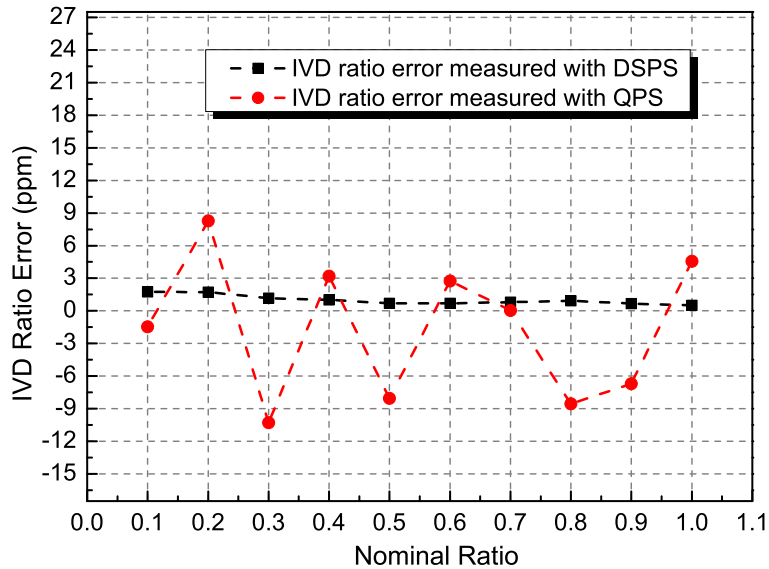


Figure 12: IVD ratio error at different taps measured with the QSP and DSPS systems.

6. Conclusion and future work

In this paper, we demonstrated the full operation of a new quantum voltage standard, built around a commercial 1 V PJVS array, developed at INRiM for the synthesis of staircase sinusoidal waveforms. All the PJVS segments have been successfully tested using a home-made short cryoprobe designed for working in a small liquid helium dewar. Quantization tests have

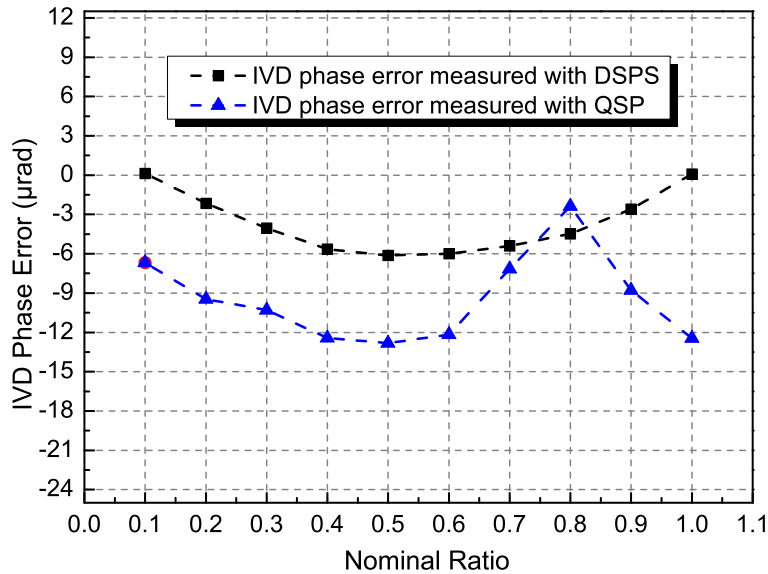


Figure 13: IVD phase error at different taps measured with the QSP and DSPS systems.

been carried out in both DC and AC regimes, demonstrating that the PJVS is working properly.

The integration of the PJVS into the sampling power standard has been completed and accompanied with the installation of a synchronous QP-multiplexer. A preliminary campaign of measurements using an inductive voltage divider as a voltage ratio transfer standard has been conducted for its validation against the INRiM digital sampling power standard at 50 Hz and 800 mV. First comparison measurements show differences in terms of IVD ration and phase errors between both QPS and DSPS setups within 12 ppm. The results demonstrate that the QPS is running properly, but further experimental investigations are in progress to identify possible sources of systematic errors to mitigate the aforementioned differences.

In the near future, a comparison will take place among the project part-

ners, during which different QPS implementations will be validated as a whole including also voltage and current transducers.

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