Non-Conventional PJVS Exploiting First and Second Steps to Reduce Junctions and Bias Lines

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Paolo Durandetto, and Andrea Sosso

***Abstract*—Quantum Digital-to-Analog Converters (DACs) based on programmable Josephson array (PJVS) represent the most widely used quantum standard in ac voltage calibrations. The extension of PJVS frequency above the kHz range appears to be arduous, yet some enhancement are still practicable. In this work we demonstrate the possibility to advantageously operate a conventional binary-divided PJVS array with a reduced number of bias lines. This feature is achieved by exploiting both first and second Shapiro steps along with non-conventional DAC codings. Two newly devised bias techniques are described in detail and preliminary experimental tests on waveform synthesis have been carried out and are presented here.**

***Index Terms*—Programmable Josephson array, ac voltage metrology, biasing.**

I. Introduction

The Programmable Josephson Voltage Standard (PJVS) is a remarkable outcome of superconducting electronics developed in the last decades [1]. This technology eventually evolved in the ac quantum voltmeter, a commercially-available calibration system that enables the measurement of ac voltages with ultimate accuracy through differential sampling [2], [3]. Investigation on PJVS seems to have reached a stable point, since most of the efforts in this field are nowadays addressed to the improvement of the pulse-driven Josephson voltage standard [4], also known as Josephson Arbitrary Waveform Synthesizer (JAWS), because of its capability of synthesizing very pure voltage waveforms up to the MHz range [5]. It is universally recognized that the major issue of PJVSs derives from its stepwise nature: during transients in step switching, the array is not quantized and the voltage unpredictable. Additionally, fast switching of the employed bias electronics may introduce interfering signals [6]. Although a solution to this limitation was found with the sampling technique, the upper operating frequency is limited to a few kilohertz. However, some interesting advancements are still possible [7], [8].

In this paper we present new unconventional bias methods to reduce the number of Josephson junctions and bias lines per volt by exploiting both first and second Shapiro steps [9]. First, a description of these new implemented bias techniques is given, with some details of the mathematical principles that support the proposed methods. Subsequently, an analysis of the proper experimental conditions, in particular power and temperature requirements, for the optimal operation of both first and second quantum steps is presented. Finally, the results of first experimental tests performed in cryocooler with a modified conventional 1 V PJVS array are reported.

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II. Balanced ternary PJVS

As known, common binary-divided PJVSs are based on a two-level codification with digits 0 and 1. Nevertheless, three quantum steps are available, namely $n = -1, 0$ and 1, where 0 and +1 (-1) steps are exploited for generating positive (negative) output voltages. Yet, these three accessible quantum steps are not fully exploited in binary-divided arrays, whose code is redundant, i.e. a generic output voltage V_{out} is obtained with different binary encodings, where sections with positive and negative steps sum up to the same value. In order to get rid of redundancy in PJVSs, a ternary structure of the sub-arrays can be adopted. Since the three quantum levels are symmetric with respect to zero, this ternary DAC is said to be balanced. A clear advantage of ternary encoding is the absence of the "wasted code" of binary, i.e. more than one digits combination can be used to represent a given number, with several beneficial consequences like fewer bias lines and junctions per volt (or, reciprocally, higher array resolution). PJVSs with a ternary structure were first fabricated and employed by researchers of National Institute of Standards and Technology (NIST) [10], [11], [12], [13].

A comparison between binary and balanced ternary PJVSs exploiting $n = 0$ and ± 1 quantum steps is provided in Tab. I, considering arrays capable of providing at least 1 V.

For an excitation frequency f_{rf} = 70 GHz, the voltage across a single junction is $V_{LSB} \simeq 145\,\mu V$, which represents

TABLE I
Comparison between conventional binary and balanced ternary PJVSs. Data are provided for arrays capable of generating at least 1 V at 70 GHz with Shapiro steps up to the first order. The third line lists the Shapiro steps required to encode positive voltages. For negative voltages, these are reversed.

	Binary	**Balanced ternary**
Number of Josephson junctions N_{JJ}	8191	9841
Number of sub-arrays m	13	9
Steps order n for $V_{out} \geq 0$	0, +1	-1, 0, +1
Full-scale voltage V_{FS} ($f_{rf} = 70$ GHz)	1.186 V	1.425 V
Redundancy	yes	no

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the resolution of the PJVS DAC. Therefore, number of digits and of Josephson junctions should be calculated accordingly to obtain the desired output voltage V_{out}.

To that aim, we first calculate the number of digits (i.e. the number of sub-arrays and bias lines) as the minimum integer value m that satisfies:

$$h \cdot V_{LSB} \cdot \sum_{i=0}^{m-1} b^i \geq V_{out} \tag{1}$$

where b and h are codification base and highest available quantum step ($b = 2$ or 3, $h = 1$, in this case). After few mathematical manipulations and taking advantage of the geometric progression property:

$$\sum_{i=0}^{m-1} b^i = \frac{b^m - 1}{b - 1} \tag{2}$$

it can be found that

$$m = \left\lceil \log_b \left(\frac{V_{out}}{V_{LSB}} \cdot \frac{b-1}{h} + 1 \right) \right\rceil \tag{3}$$

where $\lceil \rceil$ is the ceiling operator. Finally, number of junctions N_{JJ} and full-scale voltage V_{FS} are calculated as

$$N_{JJ} = \frac{b^m - 1}{b - 1} \tag{4}$$

$$V_{FS} = h \cdot N_{JJ} \cdot V_{LSB} \tag{5}$$

It has to be noted from Tab. I that only nine independent sub-arrays are needed for the 1 V balanced ternary array and, consequently, four fewer bias lines are required to current-drive it, at the expenses of a small increase of the total number of junctions.

III. Exploiting first and second quantum steps

A further reduction of Josephson junctions and bias channels can be achieved with more digit-levels, for instance by using $n = \pm 2$ steps, in addition to zero and first quantum levels. In particular, the possibility of having large $n = 0, 1$ and 2 steps provides a wider range of choices for the base number b.

We present here new methods taking advantage of this approach, which are convenient in terms of voltage resolution, full-scale and instrumentation requirements.

A. Doubling PJVS output voltage

A straightforward advancement that can be obtained from the availability of second order Shapiro steps is the increase of the maximum output voltage. This idea has been already exploited for both PJVS [14] and JAWS arrays [15], [16]. In [14], both full-scale voltage V_{FS} and resolution V_{LSB} were doubled using a 13-bit PJVS made by superconductor-normal metal-insulator-superconductor (SNIS) junctions [17].

Conversely, we propose here a new approach that doubles V_{FS}, leaving V_{LSB} equal to the $n = 1$ case. This can be accomplished exploiting both first and second order steps and by modifying the bias currents calculation algorithm in order to take advantage of the availability of the second voltage level.

TABLE II
Comparison between a conventional 14-bit PJVS and a "virtual" 14-bit PJVS exploiting both first and second quantum steps. The third line lists the Shapiro steps required to encode positive voltages. For negative voltages, these are reversed.

	Conventional	***Virtual***
Number of Josephson junctions N_{JJ}	16 383	8191
Number of sub-arrays m	14	13
Steps order n for $V_{out} \geq 0$	0, +1	0, +1, +2
Full-scale voltage V_{FS} ($f_{rf} = 70$ GHz)	2.371 V	2.371 V

This approach is formally not different from adding one more digit to the original PJVS sequence. In the conventional binary-mode (where $n = 0$ and 1), this is achieved by physically adding another individually-biased sub-array, hence doubling the effective number of junctions. On the other hand, exploiting second quantum steps, a further bit (named *virtual* in the following) can be used, for which no additional junctions and dedicated bias channel are requested, as shown in Tab. II in the case of a 14-bit PJVS.

The existence of the virtual most significant bit allows a reduction of one bias line and half of the Josephson junctions, compared to a conventional PJVS with fourteen sub-arrays (i.e. physical bits), that are the minimum required for reaching a voltage output of at least 2 V at 70 GHz.

B. Non-binary PJVS

If $n = 0, \pm 1$ and ± 2 quantum steps are simultaneously available, codification bases up to five can be exploited. Non-binary PJVS DACs main parameters for $V_{out} \geq 1$ V are listed in Tab. III, where digits, number of junctions and full-scale voltages are calculated via Eqs. 3, 4 and 5 with $b = 3, 4$ or 5 and $h = 2$. As expected, balanced-quinary PJVS represents the most convenient arrangement: compared to conventional binary PJVS, it would allow a reduction in the number of junctions and bias lines by more than a factor of two.

Concerning ternary arrays, it can be noted that there is no difference between balanced (with $n = 0$ and ± 1, Tab. I) and unbalanced versions (with $n = 0, \pm 1$ and ± 2, Tab. III), because the same numbers of junctions and sub-arrays for achieving the 1 V level at 70 GHz are needed. However, V_{FS} is doubled for the unbalanced one, due to the fact that second quantum steps are used.

Owing to the present unavailability of PJVSs with $b > 3$, we devised a bias technique where the conventional binary array is treated as quaternary, namely using only the subsections counting power-of-four number of junctions [1, 4, 16, 64, ...], as sketched in Fig. 1. Positive output voltages are obtained by current-biasing the subsections on the n step, where n is properly chosen among -1, 0, +1 and +2. For negative voltages, quantum steps -2, -1, 0 and +1 are used instead. Thus, bipolar

TABLE III

COMPARISON BETWEEN UNBALANCED TERNARY, "PARTIALLY-BALANCED" QUATERNARY AND BALANCED QUINARY PJVSS. DATA ARE PROVIDED FOR ARRAYS CAPABLE OF GENERATING AT LEAST 1 V AT 70 GHZ WITH SHAPIRO STEPS UP TO THE SECOND ORDER. THE THIRD LINE LISTS THE SHAPIRO STEPS REQUIRED TO ENCODE POSITIVE VOLTAGES. FOR NEGATIVE VOLTAGES, THESE ARE REVERSED.

	Unbalanced ternary	***Partially-balanced* quaternary**	**Balanced quinary**
Number of Josephson junctions N_{JJ}	9841	5461	3906
Number of sub-arrays m	9	7	6
Steps order n for $V_{out} \geq 0$	0, +1, +2	-1, 0, +1, +2	-2, -1, 0, +1, +2
Full-scale voltage V_{FS} ($f_{rf} = 70\,\mathrm{GHz}$)	2.849 V	1.581 V	1.131 V
Redundancy	yes	yes	no

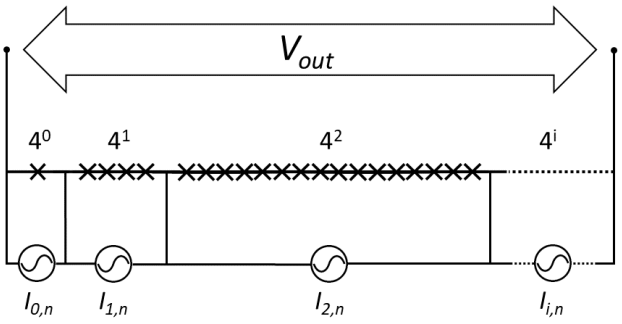

Fig. 1. Schematic circuit of the quaternary-divided array with Shapiro step order $n = 0, \pm 1$ and ± 2.

waveforms with quaternary arrays actually need all the five quantum voltages, exhibiting a redundant condition similar to that of binary-divided arrays, which use three quantum levels (-1, 0 and +1) to synthesize bipolar waveforms. The alternate four voltage levels exploited by such quaternary-divided array are quasi-symmetric with respect to the zero-level, so we refer to it as *partially-balanced* quaternary PJVS.

From Tab. III, it can be deduced that the presence of both first and second quantum steps is beneficial in terms of required number of junctions and bias lines. Furthermore, reducing PJVS size and sub-arrays would be also advantageous for the microwave transmission line, since a lower number of on-chip power-dividers and parallel striplines would be requested. Nevertheless, in order to be addressed, a partial redesign of Josephson chip should be undertaken.

C. Binary and non-binary 10 V PJVSs

Due to the recent improvements in the technology of pulse-driven Josephson devices, the synthesis of spectrally pure ac voltage signals at 1 V and higher has been demonstrated [18], [19]. Owing to the high-purity of these quantum waveforms, it is expected that 1 V PJVSs are going to be replaced by JAWS standards. Yet, JAWS voltages are still far from the 10 V level, which is one of the major breakthrough of PJVS technology [20], [21]. For this reason, it is interesting to know how the availability of five quantum voltage steps would affect the 10 V PJVS standards.

As for the 1 V scenario, using Eqs. 3, 4 and 5 one can find the number of sub-arrays m and junctions N_{JJ} required for obtaining a voltage V_{out} of at least 10 V, for a given rf frequency. This tenfold increase of V_{out} leads unavoidably to the need of additional digits, physically represented by larger sub-arrays, which may cause the total number of junctions to considerably exceed the 10 V threshold ($V_{FS} \gg V_{out} = 10\,\mathrm{V}$). For example, this situation actually occurs for binary and balanced-quinary PJVSs driven at 70 GHz, for which the full-scale voltage turns to be almost twice and three times the 10 V target voltage, respectively (see Tab. IV).

It is clear the that adopting exact base b sequences may not be favorable. However, there are several ways to arrange m sub-arrays in "quasi-exact" base b series, as a way of minimizing the number of junctions necessary to reach the V_{out} threshold, at the expenses of the system redundancy. The simplest possibility is to replace the largest segment with one containing a number of junctions N^* sufficient to meet the V_{out} requirement.

A more elegant solution is to take N^* as a power-of-b number, hence $N^* = b^k$, with the exponent k calculated as

$$k = \left\lceil \log_b \left(\frac{V_{out}}{h} - \frac{b^{m-1} - 1}{b - 1} V_{LSB} \right) \right\rceil \tag{6}$$

These N^* junctions are then split in $k + 1$ parts according to

$$N^* = b^k = 1 + \sum_{i=0}^{k-1} (b - 1)\, b^i \tag{7}$$

and the k elements of the summation are distributed one-by-one among the last k of the $m - 1$ sub-arrays. For not affecting the resolution, the single junction in Eq. 7 is included as additional sub-array, thus bringing the total number of segments again to m. Using this approach, the junctions result to be organized in m sub-arrays as follows

$$\begin{aligned} [N_0, N_1, ..., N_{m-2}, N_{m-1}] = \\ = [N_0] + [N_1] + ... + [N_{m-2}] + [N_{m-1}] = \\ = [1] + \sum_{i=0}^{j-1} [b^i] + \sum_{i=j}^{m-2} [\alpha\, b^i] \end{aligned} \tag{8}$$

with $j = m - k - 1$ and $\alpha = 1 + (b - 1)/b^j$.

From Eq. 8, it can be seen that basically two distinct base b sequences are present: the first one (with sub-arrays from 0 to $j - 1$) follows a normal progression, while the second one (with sub-arrays from j to $m - 2$) is α-weighted. As already mentioned, the first single junction (N_0) "fixes" the resolution.

TABLE IV
COMPARISON BETWEEN EXACT-BINARY, EXACT-QUINARY, QUASI-BINARY AND QUASI-QUINARY 10 V PJVSS AT 70 GHZ. THE THIRD LINE LISTS THE SHAPIRO STEPS REQUIRED TO ENCODE POSITIVE VOLTAGES. FOR NEGATIVE VOLTAGES, THESE ARE REVERSED.

	Exact-binary	**Exact-quinary**	**Quasi-binary**	**Quasi-quinary**
Number of Josephson junctions N_{JJ}	131 071	97 656	69 631	35 156
Number of sub-arrays m	17	8	17	8
Steps order n for $V_{out} \geq 0$	0, +1	-2, -1, 0, +1, +2	0, +1	-2, -1, 0, +1, +2
Full-scale voltage V_{FS} ($f_{rf} = 70$ GHz)	18.97 V	28.27 V	10.08 V	10.18 V

Quasi-binary 10 V PJVSs following Eq. 8 have being fabricated and employed for years at Physikalisch-Technische Bundesanstalt (PTB) [21]: here the sequence is exactly binary for the first four segments ($i < j = 4$), giving [1, 2, 4, 8], whereas the following sub-arrays are rescaled by $\alpha = 17/16$, thus starting the second binary series [17, 34, 68, ..., 34 816]. Similar scenarios result for $b > 2$: as an example, for a 10 V quasi-quinary PJVS, $j = 1$, $\alpha = 9/5$ and the final sequence becomes [1, 1, 9, 45, 225, ..., 28 125].

Tab. IV summarizes and compares the main parameters of exact-binary and quinary PJVSs that follow from Eqs. 3 to 5 and their quasi-exact sequence versions obtained with Eqs. 6 to 8. Besides the aforementioned spare of junctions from perfect to quasi-exact sequences, Tab. IV highlights that exploiting first and second quantum steps in 10 V quasi-quinary PJVSs leads to a significant decrease of bias lines number (from seventeen to eight), though, as will be discussed in Section IV-B, with a theoretical reduction of quantum margins above 40 %.

IV. OPERATING CONDITIONS TO OPTIMIZE BOTH FIRST AND SECOND SHAPIRO STEPS

In order to guarantee adequate operating margins and noise immunity, step amplitudes ΔI_n should be as high as possible. Generally, a quantum-range of at least 500 µA is desired [22]. With the aim of attaining simultaneously large ΔI_0, ΔI_1 and ΔI_2 values, fundamentals parameters as temperature and rf power should be set to meet the conditions described as follows.

A. Josephson junction temperature

As known, Shapiro steps of order n are enhanced when $n \cdot f_{rf} \simeq f_c$, where f_c is the Josephson characteristic frequency. Hence, in the conventional method where first Shapiro steps are exploited, the characteristic frequency should exhibit a value close to the excitation frequency f_{rf} [17]. On the other hand, higher order voltage steps are enhanced for larger f_c values. The characteristic frequency is directly related to junctions electrical parameters via the relation $f_c = K_J \cdot V_c$, with K_J indicating the Josephson constant and where the junction characteristic voltage V_c is calculated as the product of critical current I_c and normal resistance R_n. Therefore, the optimization of V_c and, consequently, of f_c is achieved by properly trimming I_c and R_n values. For a typical driving frequency of 70 GHz, $V_c \simeq 145$ µV, which represents the optimal value for getting wide $n = \pm 1$ Shapiro steps. In order to enhance rf coupling [23] with the second Josephson harmonic ($n = \pm 2$), V_c should be doubled (~ 290 µV), usually by lowering the operating temperature as a way to increase critical current and characteristic voltage values. It is clear that, for achieving sufficiently wide operating margins for both first and second steps, V_c should be set to a value between 145 µV and 290 µV.

Generally, Josephson junctions are designed to be operated at 4.2 K in liquid helium, thus electrical parameters are adjusted to have $V_c \sim 145$ µV at this temperature. In this case the only way to increase V_c is to lower the operating temperature, a complicated task when working with liquid helium dewars. Properly designed cryogen-free systems represent a simpler way to cool Josephson arrays below the liquid helium boiling point, although power dissipation becomes an issue in the cryocooler's vacuum environment when such low temperatures are approached. A more straightforward solution is to employ junctions with higher characteristic voltage [24] and adjust their operating temperature via a thermo-controlled closed-loop system. A cryocooler system is particularly suitable for this [25].

B. Rf power requirements

Shapiro step amplitudes ΔI_n of a Josephson junction radiated at $f_{rf} = f_c$ are theoretically described by the relation

$$\Delta I_n = 2I_c \left| J_n \left(\frac{K_J \cdot V_{rf}}{f_{rf}} \right) \right| \tag{9}$$

where J_n are the n-th order Bessel functions of first kind and V_{rf} denotes the amplitude of the rf voltage across the junction [26]. According to Eq. 9, step amplitudes for $n = 0, 1$ and 2 are obtained and plotted in Fig. 2 as a function of the rf power. It is evident that, for a given I_c, i.e. for a fixed operating temperature, a 50 % increase of the optimal power per junction for $n = 0$ and 1 (orange shaded area) is required to get an acceptable amplitude for $n = 2$ step too (green shaded area). It can be also noted that the simultaneous optimization of three Shapiro steps leads to a significant relative reduction (> 40 %) of the quantum operating margins, given by the smallest step amplitude ($\Delta I_0 = \Delta I_2 < \Delta I_1$), compared to the conventional bias mode with $n = 0$ and 1 (orange shaded area). Yet, operating margins larger than 1 mA have been widely demonstrated [20], [27], so that even a 50 % lower value would satisfy the 500 µA criterion.

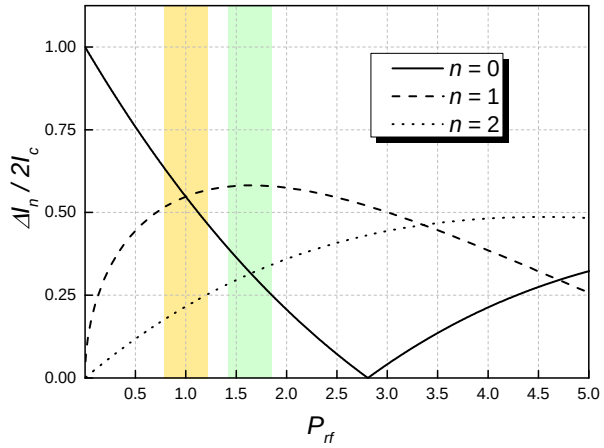

Fig. 2. Normalized Shapiro step current width for $n = 0, 1$ and 2 as a function of the rf power per junction, calculated according to Eq. 9 and knowing that $P_{rf} \propto {V_{rf}}^2$. Rf powers are normalized to the optimal P_{rf} value for getting wide $n = 0$ and 1 steps, that is the middle point of the orange shaded region. Green shaded area indicates the required rf power regions for getting simultaneously wide $n = 0, 1$ and 2 steps.

With regard to the experimental feasibility, the heat in excess can be easily dissipated both in liquid helium and in nowadays cryocoolers with cooling powers around 1 W at 4.2 K. Moreover, it should be noted that, as shown in Tab. III, the use of second quantum steps allows to decrease the number of junctions per volt by a factor of two, so that half on-chip microstriplines and power splitters are required as well. Consequently, the additional ∼50 % rf power for the simultaneous operation of 0, 1 and 2 steps discussed above should be totally compensated by the reduced number of dissipative junctions.

V. Experimental setup

Preliminary tests of the bias techniques presented in Section III have been carried out. The experimental setup included a conventional 13-bit PJVS array made of SNIS junctions [17], operated in a Cryomech PT-410[1] two-stage pulse-tube refrigerator with 1 W cooling power at 4.2 K. The PJVS chip was embedded in a special cryopackage similar to that described in [28], suitably tightened to the cryocooler coldplate (Fig. 3). A Si-diode temperature sensor, placed over the cooper bar, and a heater wire, carefully wound around the coldplate disk, are used to control and monitor the operating temperature. The excitation rf-field was supplied by a Gunn oscillator ($f_{rf} = 76.5$ GHz) and transmitted to the chip by a WR-12 stainless-steel and internally gold-plated waveguide.

To individually drive each PJVS sub-array with the required bias current, Active Technologies 1104 arbitrary voltage generators were employed. Each AT-1104 module has four independent output channels, thus four modules are needed to drive all the thirteen segments of a conventional 13-bit binary array. To that aim, a specific Python tool that remotely controls each AT-1104 module was developed and customized [29].

[1]Brand names are used for identification purposes. Such use implies neither endorsement by INRiM nor assurance that the equipment is the best available.

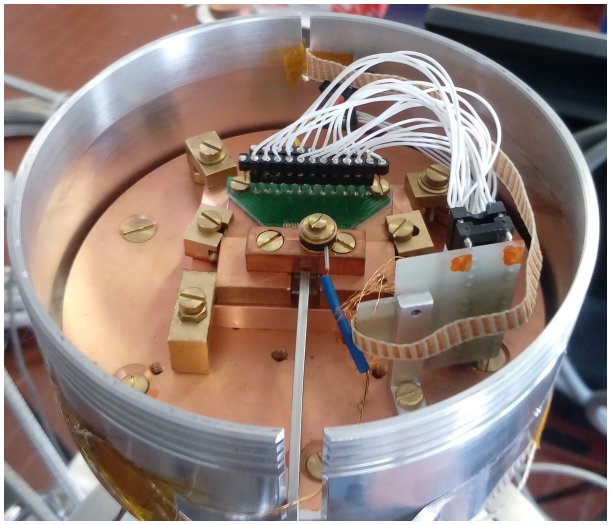

Fig. 3. PJVS sample holder mounted on the cryocooler coldplate. The Si-diode temperature sensor and the WR-12 waveguide for the rf transmission are shown as well.

As explained in Section IV-A, the operating temperature has to be set to optimize the junctions characteristic voltage V_c: at 76.5 GHz, the optimal coupling between the rf excitation and both fundamental ($n = 1$) and second harmonic ($n = 2$) Josephson oscillations occurs for $V_c \simeq 240\,\mu$V, at midpoint between f_{rf}/K_J and $2f_{rf}/K_J$. Since the PJVS chip in use exhibits $V_c \simeq 350\,\mu$V at 4.2 K, the cryocooler temperature was raised up to achieve optimal operating conditions. Around 5.2 K, $V_c \simeq 260\,\mu$V and current-voltage curves displayed in Fig. 4 were obtained. The rf power measured at the input flange is about 55 mW, which is 40 % higher than that required to optimize 0 and 1 steps at 6.5 K [14], where $V_c \simeq 155\,\mu$V. This is in line with the theoretical description presented in Section IV-B, although in that case a fixed characteristic frequency $f_c \simeq f_{rf}$ is considered. Moreover, this power value would be lower if quaternary and quinary PJVSs are

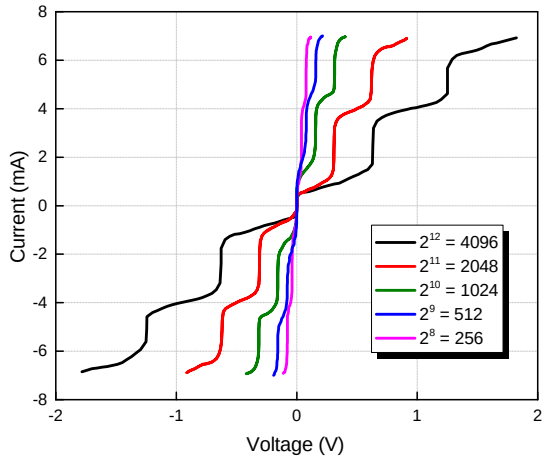

Fig. 4. Current-voltage characteristics of the five most significant bits of a 13-bit binary PJVS array under rf radiation at $T \simeq 5.2$ K in cryocooler. Both first and second Shapiro steps are visible for all subsections.

considered, as a consequence of the half number of junctions per volt.

Though quantum accurate steps were not fully achieved, partly because of the undamped cryocooler thermal fluctuations [30] ($\sim$ 350 mK at 5 K, resulting in I_c variation of approximately 500 µA), these were exploited to perform the waveform synthesis tests described in the following section.

VI. Synthesis of Stepwise Voltage Sine Waves

Tests on waveform synthesis employing the newly devised bias techniques were carried out. Proper algorithms have been developed and the main features are described in the following for two cases.

A. Sine waves with virtual 14-bit PJVS

Staircase voltage waveforms up to $V_{FS} = 2.591$ V can be synthesized adopting the bias technique presented in Section III-A. Each voltage value of the stepwise sine wave is converted into an m-size vector of digits (0, 1 or 2) that defines on which quantum step each sub-array has to be current-biased. As in the traditional PJVS operation, there are redundant ways to synthesize a generic voltage V_{out}, due to the binary structure of the array and the presence of negative quantum steps. In the following, the simplest is reported.

- For $0 \leq V_{out} \leq V_{FS}/2$, the same bias method commonly employed for conventional PJVSs is adopted. A m-size vector of only 0 and/or 1 binary-encodes V_{out}, where m is the number of physical digits ($m = 13$, in our case). Therefore, no sub-array is biased on the second quantum step.
- For $V_{FS}/2 < V_{out} \leq V_{FS}$, all sub-arrays are biased at least on $n = 1$ step, while some are biased on $n = 2$ according to needs. This is evaluated by converting $V'_{out} = V_{out} - V_{FS}/2$ into a binary m-size pattern of 0 and 1 and raising up each bit by one, thus obtaining a vector of 1 and 2. At full-scale ($V_{out} = V_{FS}$ and $V'_{out} = V_{FS}/2$), all sub-arrays are biased on the second Shapiro step.

Stepwise sine waves were synthesized at frequencies between 10 Hz and 1 kHz and amplitudes up to 2.6 V, at the operating temperature $T \sim 5.2$ K. The approximated sine wave in black shown in Fig. 5 was obtained via the conventional binary technique, thus exploiting only $n = 0$ and ± 1 Shapiro steps, since its amplitude is lower than $V_{FS}/2$. In the 2 V sine wave (red curve), second quantum steps were exploited as well, hence taking advantage of the additional *virtual* bit.

B. Sine waves with quaternary PJVS

Quaternary-divided arrays can be derived from binary ones by employing only subsections counting a number of junctions equal to an even power of two ($2^0 = 4^0$, $2^2 = 4^1$, $2^4 = 4^2$, etc.). This feature can be attained in two different ways:

1) *Fake*-quaternary: all subsections of the binary-divided array are electrically connected, hence thirteen output voltage channels (i.e. four AT-1104 modules) are actually employed for our 13-bit PJVS. No current should flow into any odd-positioned sub-array and AWGs voltage outputs are calculated accordingly. A generic quantum voltage V_{out} is then encoded into a partially-balanced quaternary digit-word $(q_7, 0, q_6, 0, q_5, 0, ..., q_1, 0, q_0)$, with $q_i = -1, 0, +1$ or $+2$ for $V_{out} \geq 0$, and $q_i = -2, -1, 0$ or $+1$ for $V_{out} < 0$.

2) *Real*-quaternary: odd-positioned PJVS sub-arrays are physically bypassed with a low (or, even better, zero) resistance short-circuit. Any voltage V_{out} can be encoded into a bit sequence $(q_7, q_6, q_5, ..., q_1, q_0)$, with $q_i = -1, 0, +1$ or $+2$ for $V_{out} \geq 0$, and $q_i = -2, -1, 0$ or $+1$ for $V_{out} < 0$. Hence, half AWG channels (only two AT-1104 modules) are actually employed with respect of the conventional bias mode.

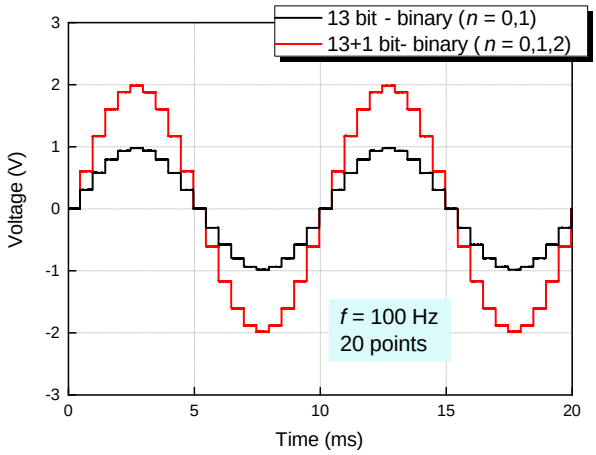

Fig. 5. Stepwise sine waves synthesized with the PJVS array in cryocooler at $T \sim 5.2$ K. The 1 V sine wave (black) was obtained with the conventional 13-bit binary technique. The 2 V sine wave (red) was obtained with the *virtual* 14-bit binary technique.

We realized the physical bypassing for the real-quaternary mode by means of short aluminum wires, wedge-bonded on the accessible pads of the chip, with an estimated electrical resistance of few mΩ at low temperature. Since bias currents are in the mA-range, a *parasitic* voltage drop up to 10 µV may occur. Although this is not negligible for ultimate metrological purposes, it does not represent a limitation in this case, which is intended as an experimental proof of concept.

The digitization of a defined voltage $V_{out} \geq 0$ in terms of a partially-balanced quaternary vector (pbq) with -1, 0, 1 and 2 digit values is derived from its unbalanced base-4 representation (uq), where only positive digit levels are used (0, 1, 2 and 3). Starting from the LSB, the non-accessible voltage levels ($n = 3$) are replaced by -1, and the left digit is increased by one, using ordinary rules of carryover additions. For example:

$$(...\,1\,3\,3)_{uq} \rightarrow (...\,1^{(+1)}\ \text{-}1^{(+1)}\ \text{-}1) \rightarrow (...\,2\ \ 0\ \ \text{-}1)_{pbq} \qquad (10)$$

where the apex terms are the carryovers. For $V_{out} < 0$, digit values are simply reversed. Applying these two quaternary bias

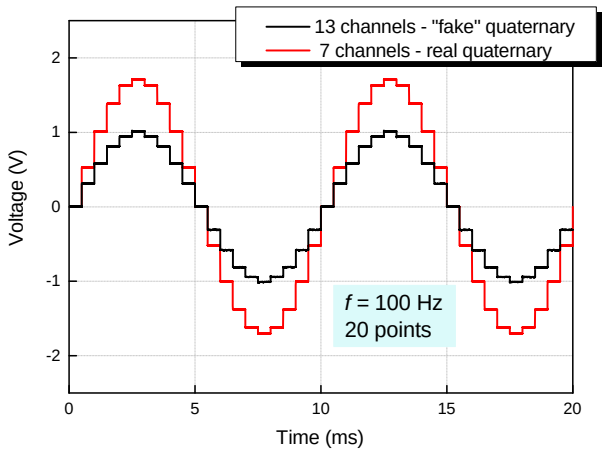

Fig. 6. Stepwise sine waves synthesized with the PJVS array in cryocooler at $T \sim 5.2\,\mathrm{K}$. The 1 V sine wave (black) was obtained with the *fake* quaternary technique. The 1.728 V sine wave (red) was obtained with the real quaternary technique.

modes, staircase approximated sinusoids were synthesized. Two 100 Hz sine waves are shown in Fig. 6.

VII. Conclusion

Possible improvements to the state-of-art of programmable Josephson array technology were presented. In particular, we proposed to simultaneously exploit first and second Shapiro steps to reduce the number of chip junctions and bias lines up to a factor of two. Using all available quantized voltage steps ($n = 0, \pm 1$ and ± 2) allows to encode a generic output voltage in a more convenient way with respect to the conventional binary codification. Such new encodings have been implemented and tested on a 13-bit 1 V PJVS operated in a pulse-tube cryocooler. However, in order to make full use of this characteristic, a partial redesign of the PJVS chip structure should be undertaken. This feasibility study is intended to be a starting point of a potential reassessment of some important features of the current PJVS that, though widely and successfully used, can still be optimized.

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